January 2012

Chemical Mechanical Planarization of Electronic Materials

Fnu Atiquzzaman
University of South Florida, atiquzzaman@mail.usf.edu

Chemical Mechanical Planarization of Electronic Materials

by

FNU Atiquzzaman

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science
Department of Mechanical Engineering
College of Engineering
University of South Florida

Co-Major Professor: Ashok Kumar, Ph.D.
Co-Major Professor: Rajiv Dubey, Ph.D.
Manoj K. Ram, Ph.D.
Rasim Guldiken, Ph.D.
Nathan Crane, Ph.D.

Date of Approval:
October 17, 2012

Keywords: Semiconductor Process, Slurry, CVD, Thin-Films Processing, Metrology

DEDICATION

This thesis is dedicated to my parents, siblings, and friends.

ACKNOWLEDGMENTS

First and foremost, I would like to thank my advisor Dr. Ashok Kumar for his supervision and help during my entire research work. I express my sincere gratitude to Dr. Rajiv Dubey for serving as a co-major professor in my thesis committee. I am grateful to Dr. Manoj K. Ram for his suggestions and constant encouragement during my work. This thesis would not be completed without support from my committee members: Dr. Rasim Guldiken and Dr. Nathan Crane. In addition, I am quite thankful to Nano Materials Research Laboratory (NMRL) members, and Nanotechnology Research and Education Center (NREC) staffs for providing help in my research work. Finally, I am really thankful to Ms. Michelle Kobus and Ms. Catherine Burton for helping me in carrying out administrative work on numerous occasions.

This research was supported through National Science Foundation Grant Number: CMMI 0727320.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

In the modern semiconductor manufacturing processes, chemical mechanical planarization (CMP) has attained important processing step because of its ability to provide global planarization. CMP is the planarization technique which is used for the removal of excess material, as left over from the previous processing steps. In addition, CMP offers a uniform surface that is essential for subsequent processing steps, especially for the high resolution photolithography processes. In simpler notation, CMP is a process where a chemical reaction enhances in obtaining a planar surface through removal of the mechanical materials from a wafer.

In this study, CMP performance of three electronic materials was investigated. Chemical vapor deposited (CVD) diamond films, as a first materials, was fabricated using hot-filament chemical vapor deposition technique (HFCVD). The synthesized microcrystalline diamond (MCD) films were characterized using Raman Spectroscopy, Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), and X-ray Diffraction (XRD). The CMP performance of the MCD and nanocrystalline diamond (NCD) synthesized in Nano Materials Research Laboratory (NMRL) were investigated by using commercial slurry procured by Logitech Inc. U.K. The post-CMP characterizations of diamond films were performed by AFM in order to investigate surface roughness. The result showed the significant reduction the surface roughness of MCD films (37 nm to 15 nm) and NCD films (18 nm to 12 nm).

In addition, the CMP performance of the silicon dioxide was investigated in this research work. The novel nanodiamond-polymer based slurry was also developed by co-polymerization of N-isopropylacrylamide (NIPAM) and N,N'-methylenebisacrylamide, 3-(trimethoxysilyl) propyl methacrylate (MPS). The synthesized slurry was characterized by Transmission Electron Microscopy (TEM) for observing the dispersion of diamond particles in the polymer matrix. The investigation of silicon dioxide was carried out using conventional ceria based slurry and novel nanodiamond-polymer based slurry. The results showed excellent surface finish at the minor expense of material removal rate with nanodiamond-polymer based slurry. Also, the coefficient of friction of friction was significantly reduced by using novel nanodiamond polymer based slurry.

Lastly, CMP behavior of copper wafer was examined under different polishing conditions. The polishing was carried out using the commercial slurry procured from Cabot Microelectronics Inc., U.S. The copper wafers were characterized by AFM in order to analyze surface roughness. The results showed the reduction in average surface roughness occurred from 4.7 nm to 1.7 nm. This range of average surface roughness meets the demands of modern semiconductor industries.

CHAPTER 1:

CHEMICAL MECHANICAL PLANARIZATION (CMP)

1.1 Introduction

The semiconductor industries have been undergoing constant improvement for over six decades. However, over the last decade the development and improvement of semiconductor manufacturing technology has been rapid, particularly in the fabrication of Integrated circuits (IC). IC fabrication is divided into two categories: front end of the line (FEOL) where circuit elements are fabricated, back end of the line (BEOL) where these individual elements are joined within IC. These rapid developments have led to ever increasing demands in today's customer oriented market [1-2].

The continuous shrinkage in the device feature size and increase in current density have led to stringent requirements for ultra-smooth and ultra-flat surface during IC fabrication processes. There have been various planarization techniques that have been extensively investigated to be used as reliable and economical fabrication process technology, including doped glass reflow, hydrophobicity, spin etch planarization, spin on deposition, reactive ion etch and etch back, and chemical mechanical planarization MP). However, CMP process technology offers significant advantages over other planarization techniques in terms of its capabilities to provide excellent global planarization and applicability to a wide range of wafer surfaces. These advantages have made CMP playing critical role in today's microelectronics, semiconductors and

microelectromechanical system (MEMS) industries. Figure 1.1 shows the improvement of wiring level by using CMP process technology [2].

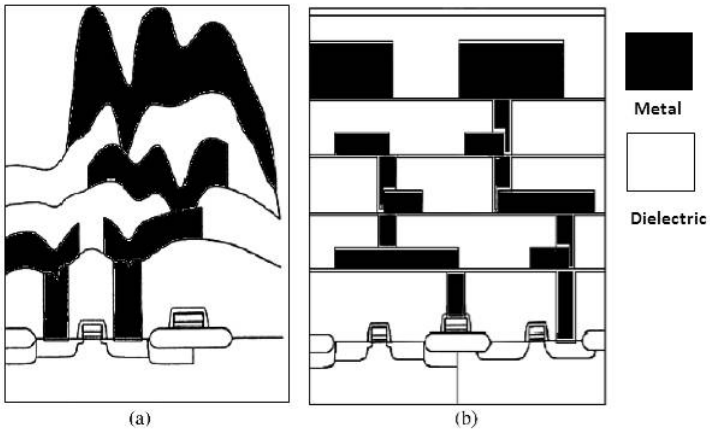

Figure 1.1 A schematic of improvement in wiring by CMP process [2]

1.2 Overview of CMP

CMP is the polishing technique used for the removal of excess material, as left over from previous processing steps. In addition, CMP offers a uniform surface that is required for subsequent processing steps, especially high resolution photolithography processes as seen in figure 1.2 [3]. In another words, CMP is a process whereby a chemical reaction enhances the mechanical material removal to get planar wafer. The schematic of CMP process is diagrammed in the figure 1.3 [4].

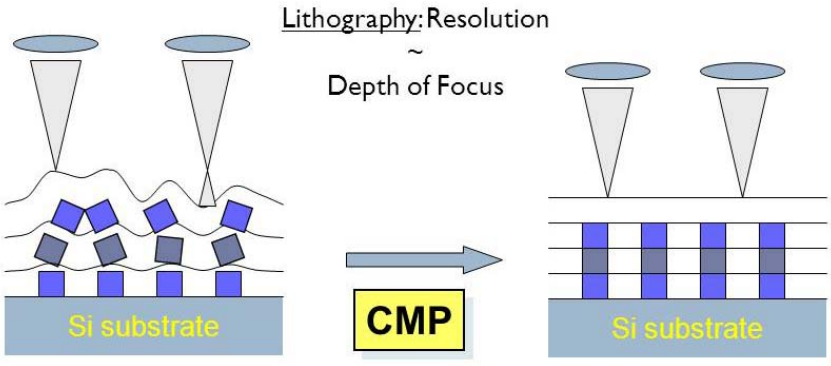

Figure 1.2 Depth of focus issue in high resolution lithography [3]

The wafer is mounted upside down between retaining rings to keep it horizontally aligned. The carrier stage has two dimensional (2D) dual force sensors, lateral positioning system, and a mechanism to provide constant pressure while pressing wafer against the polishing pad. The circular polishing pad is made to stick with a horizontal rotational drive motor capable of providing desired torque and speed during polishing. The slurry, typically a mixture of abrasive particles and chemical additives, is made to flow on the center of the pad which due the action of centrifugal force gets uniformly distributed on the entire pad surface. This helps creating a thin fluid layer across the pad surface [5].

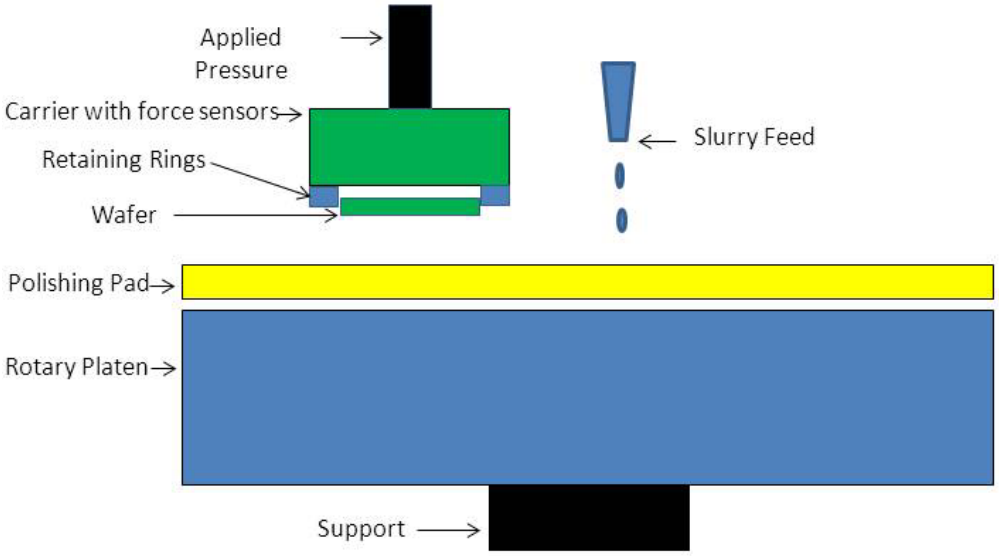

Figure 1.3 A schematic of CMP process [4]

Conditioning mechanism is a process used to soften the pad before actual polishing of wafer to enhance the polish rate and to maintain constant roughness while distributing slurry uniformly across the pad surface [5]. This process is achieved by polishing a diamond embedded mounting against the pad for certain period of time before actual polishing.

The two components mechanical and chemical occur simultaneously during CMP process and are considered to be inseparable. The mechanical action is described by the controlled speed and pressure, and that subsequently causes two body abrasion between either abrasive and wafer or abrasive and pad. The interaction between pad, abrasive and wafers are considered to be a three body abrasion system [5]. This is schematically shown in figure 1.4 [4]. On the other hand, chemical action is described by the reaction occurring between chemical reagents in slurry and wafer, which in turn results in the modification of wafer surface enhancing its removal. The chemical reagents are tailored toward a particular wafer and its characteristics to react in way that helps efficient material removal. Wafers or thin films have their own properties and chemical additives in the slurry must be designed accordingly. Besides, chemical additives assist in dissolving the abraded materials and preventing them from re-deposition onto the wafer surface. The CMP process looks simple on the surface but mechanisms associated underneath it are very complex and still lacks understanding in totality.

The material removal mechanism is often explained by the empirical equation called Preston's Law [1]:

$$MRR = K_p \times P \times V \tag{1}$$

where:

MRR – Material removal rate

K_p – Preston's constant

P – Pressure applied

V – Relative velocity of wafer surface and pad

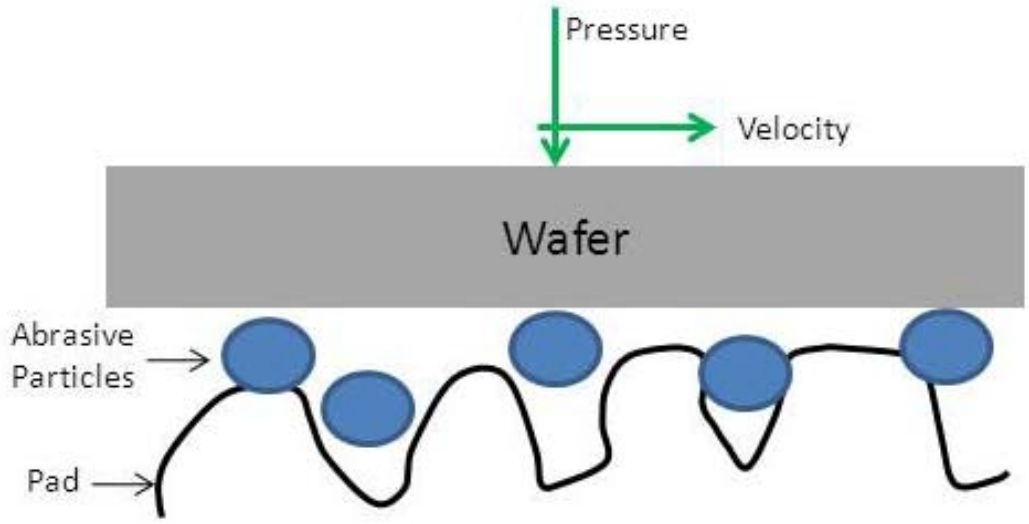

Figure 1.4 A schematic of interaction between wafer, pad and abrasive during CMP [4]

CMP was developed at IBM® Base Technology Laboratory, East Fishkill NY in the 1980s as an important processing step in IC fabrication [2]. The main purpose of the development was to use CMP technology in the production of high end multiple level metallization. For the last two decades, CMP has evolved and paved way for the development of new IC fabrication processes. Copper-interconnect technology, Shallow Trench Isolation (STI), and Tungsten polishing were developed after the advent of CMP technology. These advantages of CMP technology have made it reliable, stable and cost effective production-oriented semiconductor market place [2].

As device feature size keeps shrinking, the demand for ultrasmooth, ultraflat surface is increasing exponentially to improve the performance of the integrated circuit (IC) chips. This long-term trend is dictated by Moore's law which proposed by Intel® co-founder Gordon E. Moore in his 1965 paper [6]. According to Moore's law, "the number of transistors incorporated in a chip will approximately double every 24 months," as represented graphically in figure 1.5 [7]. This law has been valid since its inception, and

recent announcement of Intel® 22nm 3-D Tri-Gate proves that the Moore's law will continue to be hold true [8].

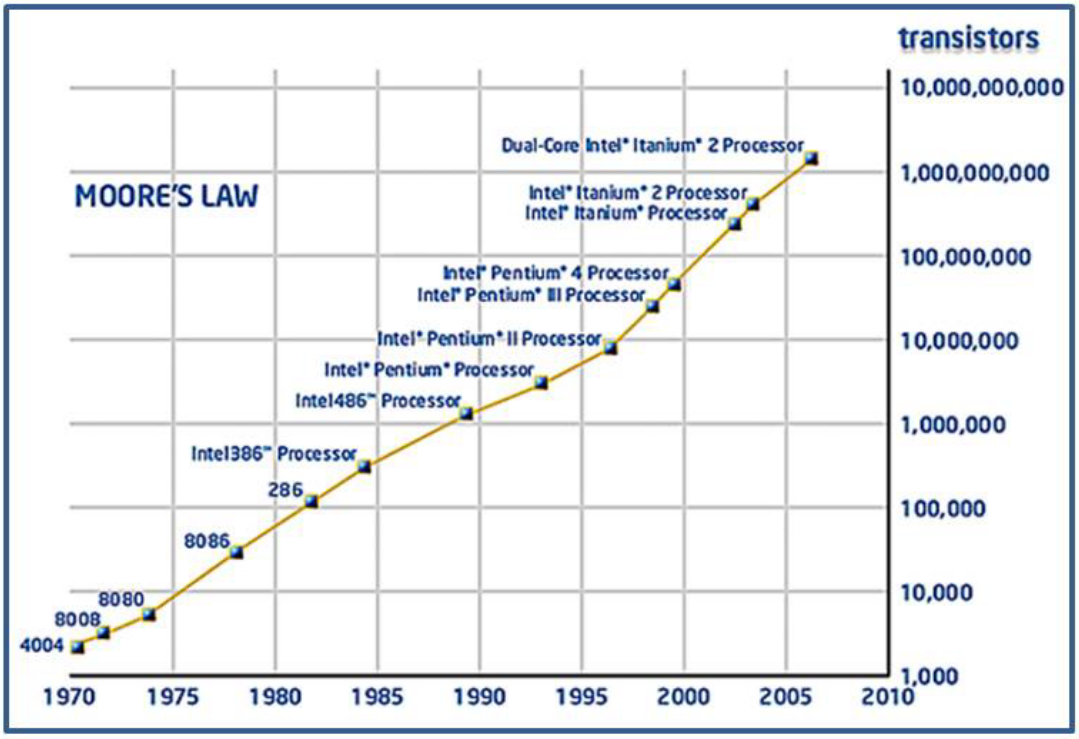

Figure 1.5 Moore's Law [7]

1.3 Types of CMP

The CMP technology can be divided into two broad categories: dielectric and polysilicon CMP, and metal CMP [4]. The comprehensive analysis of different types of CMP of electronic materials is shown in table 1.1 [1].

The following subsections provide the overview of some of the important CMP processes.

Table 1.1 List of electronic materials and their application after CMP processes [1]

	Materials	Application
Metal	Al	Interconnection
	Cu	Interconnection
	Ta	Diffusion Barrier/Adhesion Promoter
	Ti	Diffusion Barrier/Adhesion Promoter
	TiN, TiNxCy	Diffusion Barrier/Adhesion Promoter
	W	Interconnection
Dielectric	Cu-Alloys	Interconnection
	Al-Alloys	Interconnection
	Polysilicon	Gate/Interconnection
	SiO2	Inter-Level Dielectric (ILD)
	BPSG	ILD
	PSG	ILD
	Polymer	ILD
	Si3N4 or SiOxNy	Passivation/Hard CMP Stop Layer
Others	Aerogels	ILD
	ITO	Flat Panel
	High K Dielectric	Packaging/Capacitor
	High Tc Superconductor	Interconnection/Packaging
	Optoelectronic Materials	Optoelectronics
	Plastics, Ceramics	Packaging
	Silicon-on-Insulator (SOI)	Advanced Devices/Circuits

1.3.1 Inter Level Dielectric (ILD)

To make multi-level metal (MLM) structures, wafer needs to be polished after the deposition of dielectric in order to get planar surface. The higher planarity demands were raised by at least three following processing steps: photolithography, metal deposition, and metal etch after the deposition of dielectric layer [2].

A dielectric layer, typically silicon dioxide (SiO_2), is deposited over silicon substrate which has transistors built on it, in order to make multilevel wiring. The deposited oxide layer takes shape of step height underneath, which in turn results in rough topography of the surface causing difficulties in carrying out high resolution lithography as schematically represented in figure 1.2. Depth of focus issue is main reasons for hindering the lithography process and besides that, thin metal layer across the step height increases the resistance of wiring as well, which subsequently leads to problems during metal etching process. To avoid that happening, various techniques, as mentioned in section 1.1, have been investigated for their feasibility to be used as planarization techniques and CMP came out as a best technique for planarization. The schematic of ILD process is diagrammed in figure 1.6 [9], and it represents the use of CMP to achieve smooth and defect free surface for further IC fabrication steps.

Among all the CMP processes, ILD CMP closely follows Preston's Law as discussed in section 1.2. The common abrasive used in slurry for oxide polishing is silica particles and its size about 25nm for colloidal silica and about 300 nm for fumed silica. Ceria is also a commonly used abrasive for oxide polishing. The pH is maintained within range 10.5-11.5 to achieve optimized polishing condition. Silicon dioxide is highly soluble in aqueous medium forming silicon hydroxide which can be etched away by polishing as represented by following equation [1]:

$$SiO_2 + 2H_2O \rightarrow Si(OH)_4 \quad (2)$$

ILD process was the first and still the largest application of CMP technology in the IC fabrication [4].

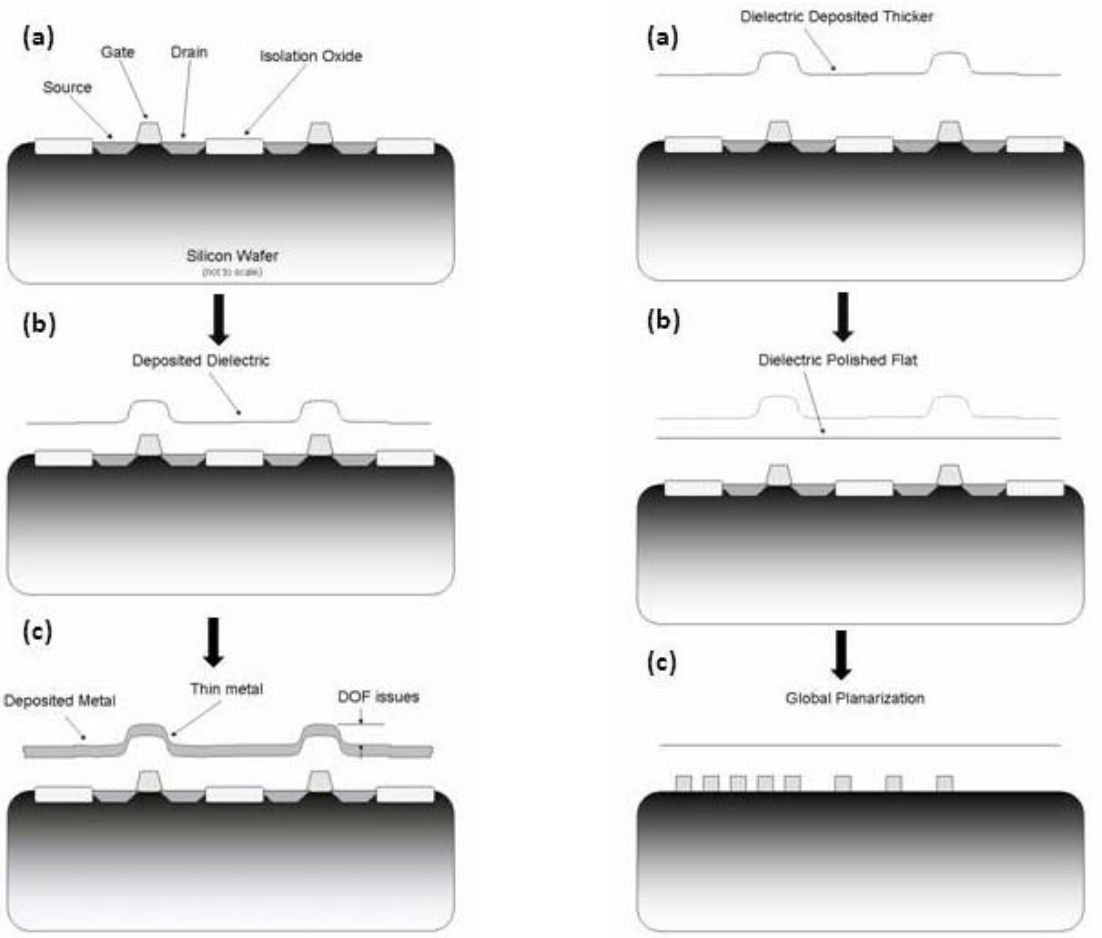

Figure 1.6 A schematic of ILD CMP process [9]

1.3.2 Metal CMP

Metal CMP, an important step in the IC fabrication, is used to fabricate "damascene" structures serving the purpose of 'wiring' that connect the individual electronic components (transistors). In current state-of-the-art IC fabrication where silicon is used as substrate material, damascene structures must be formed in order to fabricate millions of transistors over the substrate.

In a typical metal CMP process, the metal is deposited over etched dielectric layer. In most cases, a barrier layer, usually of either Ti/TiN or Ta/TaN, is deposited over

the dielectric in order to avoid metal diffusion into dielectric as diagrammed in figure 1.7 [10]. The details of deposition processes, pattering, and etching are irrelevant when talking the context of CMP, however, these processes are carried out using deep UV photolithography, etching, physical vapor deposition (PVD), chemical vapor deposition (CVD) techniques.

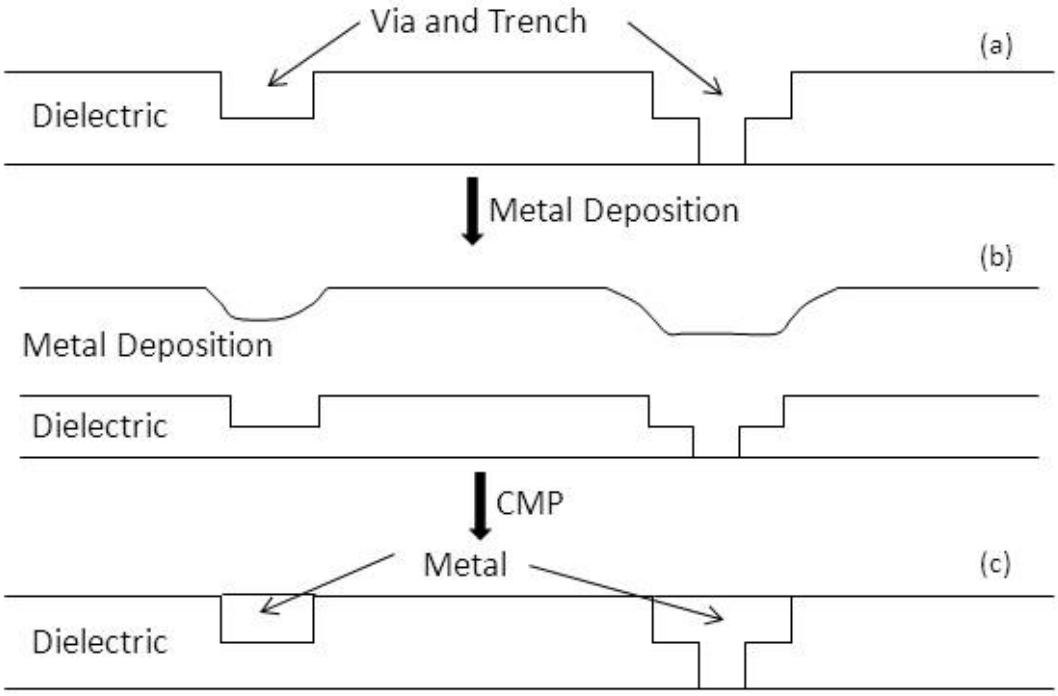

Figure 1.7 A schematic of metal CMP process [10]

1.3.3 Non-IC Application of CMP Technology

The CMP technology, after its successful implementation in the IC fabrication for more than two decades, is starting to play an important role in the fabrication of sensors, actuators, microptical devices, hard-disc drive, and other microdevices. These types of device fabrications are known as *'microfabrications'*, which signifies at least

some features of the device are in the micrometer scale range. It can also be expressed by terms such as micromaching, microelectromechanical systems (MEMS), or microsystem technology (MST) [2].

At the beginning the CMP technology is used for only making simple planarization of surface in the microfabrication, but it has become an enabling technology for making multilevel structures like gears, micrometers, etc. The market research shows the growth in sales of $12 billion in 2004 to $25 billion in 2009 [11]. This trend is continued to follow in the near future, and the CMP technology would continue to play a crucial fabrication step in the microfabrication.

1.4 Thesis Scope and Outline

1.4.1 CVD Diamond Films

Diamond is one of the most important wide bandgap semiconductors that have shown the capability to operate in extreme environments like high temperature, high pressure, high frequency, advanced laser, optoelectronics devices due to their exceptional properties [12]. Extreme properties of diamond in terms of their hardness and chemical inertness make the planarization process very difficult and still lack understanding of fundamental CMP mechanism in totality. Therefore diamond films, as a first candidate material for this thesis, have been chosen for planarization using state-of-the-art slurry for understanding the underlying mechanisms of diamond CMP process. CMP has been playing crucial role in the manufacturing of Si-based electronic devices for last couple of decades. With the advent of modern wide bandgap semiconductors to fabricate electronic

components that are used in extreme environments, CMP process needs to precisely develop for the wide bandgap semiconductor planarization.

The planar diamond film substrates are necessary for various applications including, radio frequency microelectromechanical system (RF MEMS), Si/GaN on diamond or silicon-on-insulator (SOI) technologies, nano-imprinting, optical windows and mirrors, ultra-low friction MEMS devices [13].

Traditionally, diamond films are deposited on the substrate by using a technique called chemical vapor deposition (CVD), also known as vapor-phase epitaxy (VPE), in low pressure environment. The CVD process is capable of producing high quality conformal films with required properties. In addition, the CVD process is quite suitable for depositing a wide range of films including, metals, alloys, and semiconductors with controlled stoichiometry. Fundamentally the CVD process is described by the reaction between gaseous activated species and the substrate. The gaseous species are activated by either high temperature or plasma depending on the types of CVD being used. The reaction occurring between gaseous species and the substrate is dictated by the thermodynamics and kinetics of the reaction. The schematic of the CVD process is diagrammed in figure 1.8 [14].

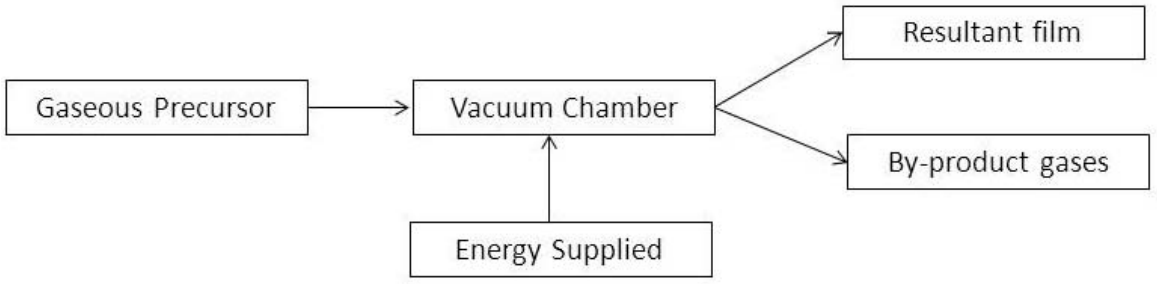

Figure 1.8 Schematic of CVD process [13]

The thermodynamics aspect represents the driving force and provides the information regarding reactants' behavior at operating temperature when they reach the substrate surface. On the other hand, kinetics represents the transport mechanism of the reactants to the substrate surface at operating temperature. As a result, deposition occurs over the substrate at the same time producing gaseous byproducts. Figure 1.9 shows a schematic of the CVD process at the atomic level [14].

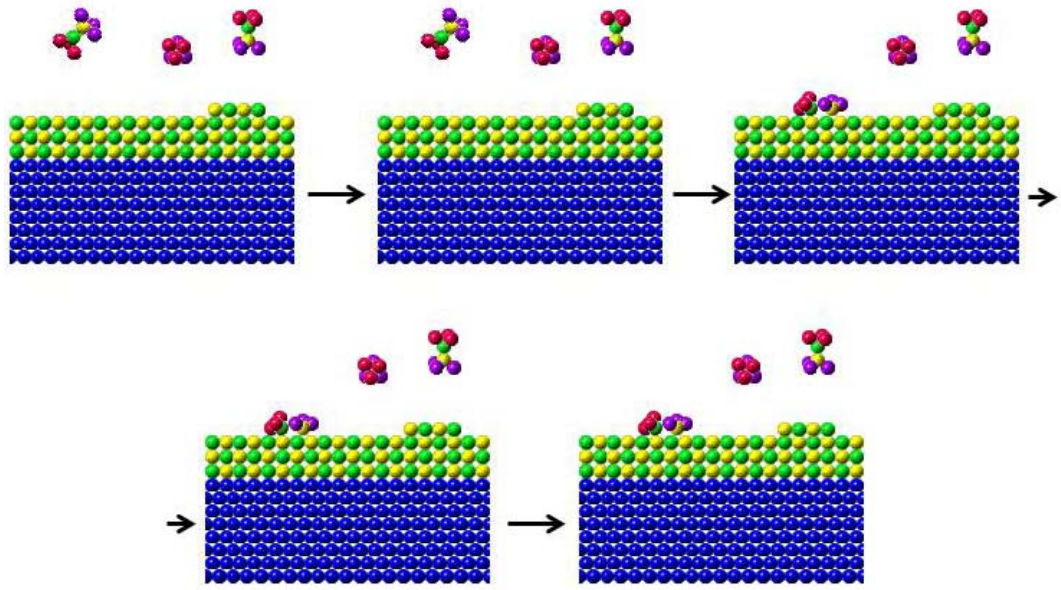

Figure 1.9 A schematic of CVD process at atomic level [14]

Diamond films are traditionally deposited on the substrate by using the technique called Chemical Vapor Deposition (CVD). CVD process for diamond deposition is divided into numerous categories based on utilized systems as follows [15].

- Hot-Filament CVD (HFCVD)
- Plasma Enhanced CVD (PECVD)
- Laser Assisted CVD (LACVD)

- Electron Assisted CVD (EACVD)]

Among the above mentioned CVD processes, the HFCVD has been used to grow diamond films for this research and will be discussed in details later section.

The chemical mechanical polishing of CVD diamond films was first demonstrated by Thornton and Wilks in 1974 [16]. They have carried out polishing by supplying a strong oxidizer solution of KNO_3 in the form of slurry between CVD diamond film and rotating disk. Since then several polishing techniques were developed by scientist and engineers in order to polish CVD diamond films. Some of the most important polishing techniques are listed below:

- Laser beam polishing [17]
- Oxidizer ($LiNO_3$ + KNO_3) enhanced polishing [18]
- Two body (diamond-diamond) abrasion [19]
- Ion-beam polishing [20]
- Abrasive water jet polishing [21]

In addition to the aforementioned techniques, a variety of techniques have been utilized to polish CVD diamond films. Recently, the development of advanced CMP processes to polish CVD diamond has gained attention from the scientific community. These processes are starting to be available commercially by companies such as Sinmat Inc. (U.S.) and Logitech Inc. (U.K.). Therefore, CMP is to play a significant role in the polishing of CVD diamond films in the near future. Therefore diamond films, as a first candidate material for this thesis, have been chosen for planarization using state-of-the-art slurry for understanding the underlying mechanisms of diamond CMP process.

1.4.2 Silicon Dioxide

Silicon dioxide is the first materials for which CMP technology was developed from glass polishing technology. In the current state-of-the-art, 40% of the total CMP processes are dedicated toward oxide polishing. With the advent of new CMP process technology like shallow trench isolation (STI), the demands have become quite stringent for the oxide polishing. During the manufacturing of the IC based devices, a wafer has to go through several oxide polishing steps at different metallization level. The current state-of-the-art involves 6-7 level of metallization with different dielectric layers. ILD CMP is supposed to polish dielectric layer after each metallization layers to achieve planarity in each layers.

The output of the polishing of dielectric layers is measured in terms of several parameters including, removal rate, within die uniformity, within-wafer uniformity, lot-to-lot uniformity, minimal surface scratches and low cost-of-ownership. These output parameters have to be optimized in order to achieve superior quality surface finish. Usually, there exists a trade-off between these optimized parameters. Recently, there has been attempt in modifying conventional abrasive particle by introducing it into the polymer matrix to enhance slurry performance during polishing. Earlier in our laboratory, Cecil ***et. al***. have synthesized ceria-polymer based microcomposites to reduce defects and scratches in oxide CMP, particularly during shallow trench isolation (STI) in logic device fabrication [22]. These synthesized particles consisted of polymer network formed from co-polymer with siloxane and acrylamide segments and interpenetrating chains of poly (acrylic acid) that functionalize ceria nanoparticles. The behavior of these synthesized ceria-polymer microcomposites was tested during the CMP of oxide

polishing. The results of these tests have shown the superior surface finish with minimal scratches due to cushioning effect provided by soft polymer matrix. In addition, the material removal rate was lowered as compared to the materials removal achieved by utilizing the ceria based slurry.

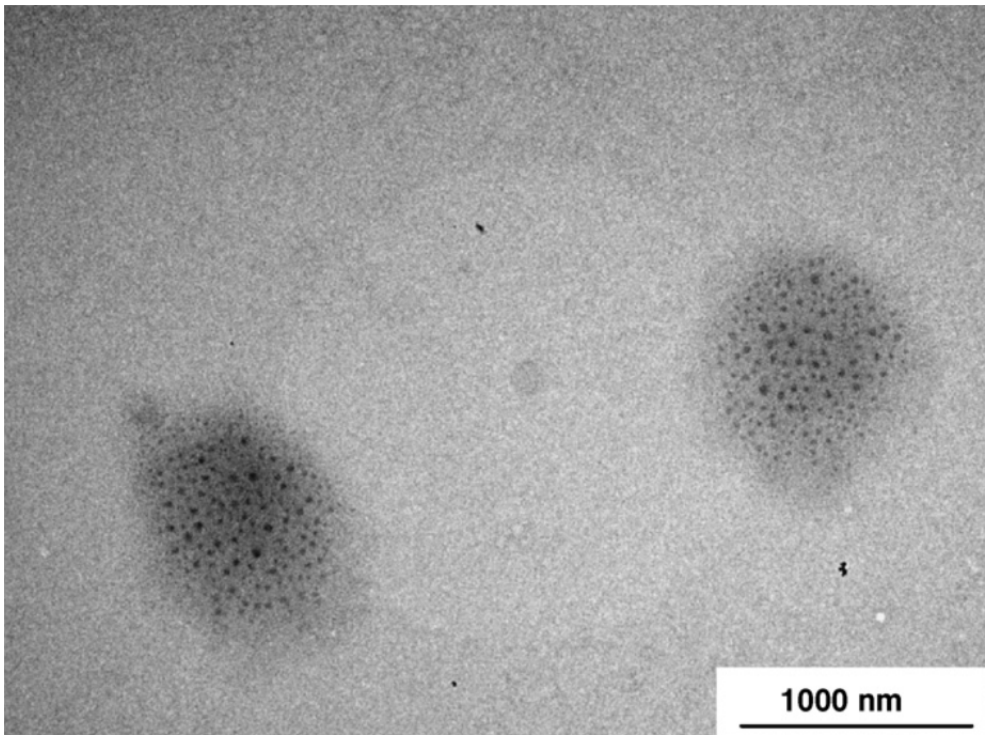

Figure 1.10 TEM image of the microcomposite particles [22]

The figure 1.10 shows the TEM image of the composite particles where dark spot represents the ceria nanoparticles [22]. It can be clearly observed from the TEM image that ceria is uniformly distributed across the polymer matrix, and this uniform distribution is responsible for providing cushioning effect during the polishing of thermally grown oxide films.

Chen et al have synthesized, characterized and investigated the oxide CMP behavior of polystyrene-core ceria-shell (PS/CeO_2) abrasives [23]. The PS/CeO_2

abrasives contain the ceria particle coated with soft organic polystyrene particles which subsequently give an advantage during polishing process. This is shown in figure 1.11 by the TEM micrograph of the synthesized PS/CeO_2 particles. It can be analyzed that the size of the PS/CeO_2 particles are 140 nm with the individual size of ceria particles are 10 nm.

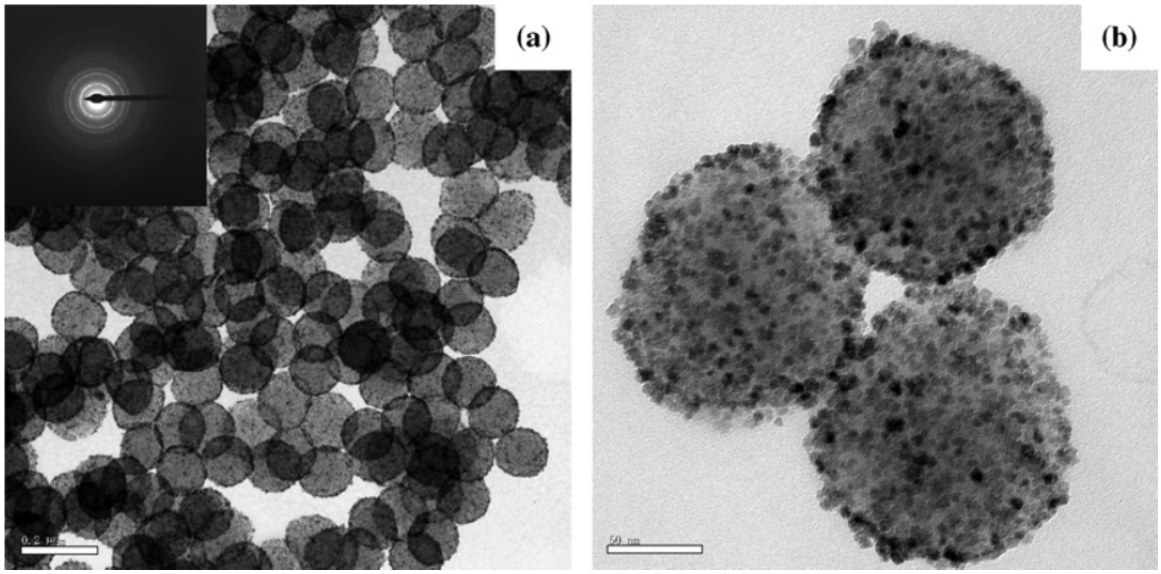

Figure 1.11 TEM image of PS/CeO_2 particles with SAED pattern [23].

Their results showed the improved thermal oxide polished surface with minimal scratches and high material removal rate. The material removal rate observed during oxide polishing by using PS/CeO_2 particles as slurry was 484.5 nm/min which is much higher than the material removal rate observed by utilizing only ceria particle which is 70.3 nm/min. These results show tremendous increase in the material removal rate during thermal oxide polishing. Silicon dioxide is chosen as a second candidate material for planarization using state-of-the-art slurry. Novel slurry based on nanodiamond and polymer composites have been synthesized and used for polishing of

silicon dioxide films. The results of planarization were compared for both commercial slurry and synthesized slurry.

1.4.3 Copper

Copper has completely replaced aluminum as an interconnect material for IC fabrication due to lower resistivity and good electromigration resistance of copper. As a result, RC delay in the ICs decreased due to excellent conductive property of copper. Table 1.2 shows the comparison between various low resistive materials [1].

Table 1.2 Properties of different metals [1]

Properties	Cu	Al	Ag	Au	W
Resistivity (μΩ-cm)	1.67	2.66	1.59	2.35	5.65
Electromigration Resistance	Good	Poor	Poor	Excellent	Excellent
Corrosion Resistance	Poor	Good	Poor	Good	Good
Adhesion to oxide layer	Poor	Good	Poor	Poor	Poor

As shown in the above table 1.2, copper has many disadvantages, and therefore additional process technologies are required to make copper as the best option for interconnects. CMP is critical to dual damascene copper interconnection technology because it removes excess materials after electroplating of copper. Copper is chosen as a third candidate material for planarization because of its wide usefulness as an interconnect materials during IC fabrication.

Copper CMP technology is complicated in a sense that slurry chemicals play an important role during the planarization process. It is common understanding that slurry chemicals first modifies the surface of the copper film by oxidizing it, and then abrasives

in the slurry removes the soft film of copper oxide on the copper surface. Therefore, it is very critical to make composition of slurry which gives proper results. Usually, a worthy copper CMP slurry must contains an oxidizer, abrasives, a chelating agent, and other additives. The commercial copper slurry must take in account various issues, including removal rate, within-wafer uniformity, slurry residue, corrosion, scratching, step height reduction, and other surface defects [2]. Hydrogen peroxide is commonly used as an oxidizing agent during copper CMP process, and it was first proposed by Hirabayashi and coworkers, they have used silica particles, hydrogen peroxide and glycine for the planarization of copper wafer [2].

1.5 Challenges in CMP of Electronic Materials

As device feature sizes and device density is decreasing, the demands for the development of new CMP technologies have increased tremendously. Following are two CMP technology developed during last few years and these are widely used for the fabrication of ICs in the semiconductor industries.

1.5.1 Shallow Trench Isolation (STI)

Shallow trench isolation (STI) is an electrical isolation technology adopted for sub-0.25 micron ICs replacing the local oxidation of silicon (LOCOS). Higher device density and efficient utilization of silicon wafer are achieved by STI. CMP is the critical part for STI fabrication during the IC manufacturing. The process flow for the STI is schematically diagrammed in figure 1.12 [24].

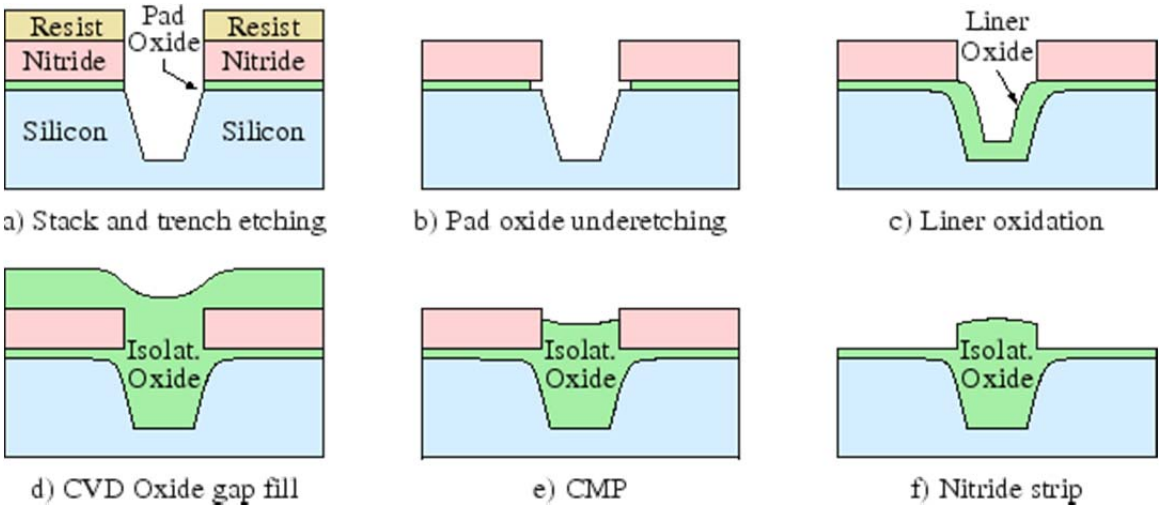

Figure 1.12 Schematic diagram of shallow trench isolation process [24]

Here, a shallow trench is made in the silicon substrate itself as seen in figure 1.12a and this is followed by the resist removal (figure 1.12) and thermal oxidation of the silicon to grow thin layer of silicon di oxide film (figure 1.12c). After the growth of thin oxide layer, chemical vapor deposition (CVD) is used for the deposition of a thick oxide film (figure 1.12d) and subsequently excess oxide films are removed by the CMP process (figure 1.12e), resulting in an isolation layer (figure 1.12f).

1.5.2 Through Silicon Via (TSV)

Through Silicon Via (TSV) is the latest technology in fabricating three dimensional (3D) device structures to maximize the packing density in order to improve performance, and keep up with Moore's Law. Semiconductor industries have long been using two dimensional (2D) packing, but now it has reached its scaling limit and made the development of 3D large scale integration (3D LSI) inevitable. The 3D LSI process is schematically shown in figure 1.13 [25].

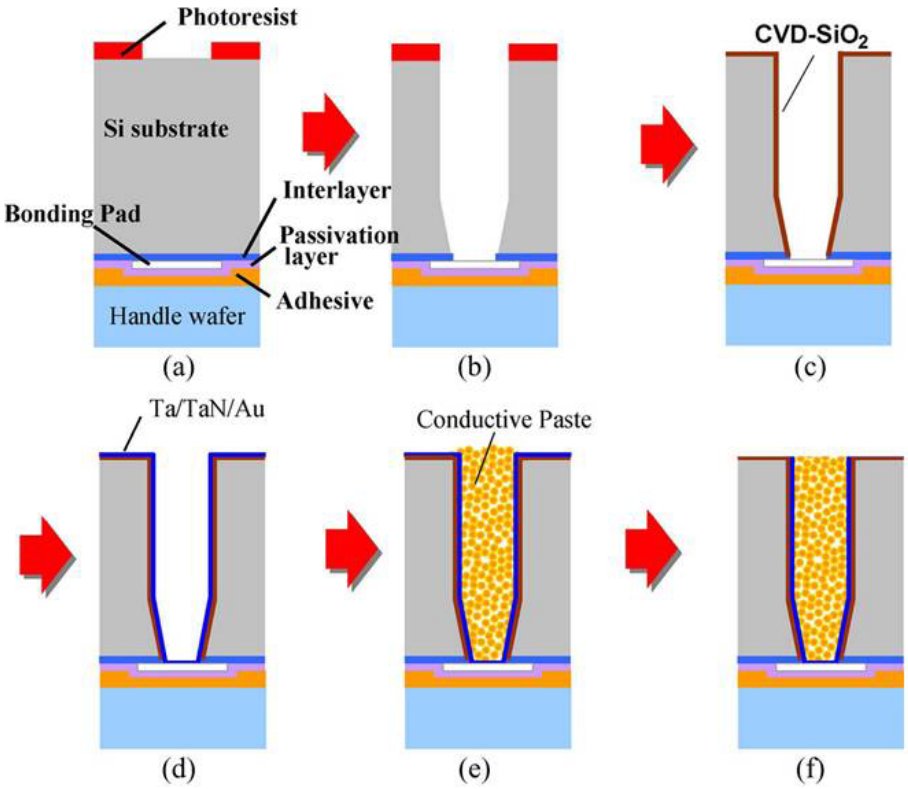

Figure 1.13 A schematic of TSV process [25]

A through hole is made by the Si etching process followed by the RIE of oxide as represented by figure 1.13a and b. In the third step, an insulating layer of SiO_2 by using low-temperature plasma-enhanced chemical vapor deposition (PECVD) process (figure 1.13c), which is followed by the deposition of a barrier layer of metal (figure 1.13d). After metal deposition, a conductive paste is used to fill the via. In the end, CMP is used to remove excess materials [2].

1.6 References

[1] J.M. Steigerwald et. al., Chemical Mechanical Planarization of Microelectronic Materials, Wiley-Interscience Publications, ISBN 0-471-13827-4, (1997).

[2] Yuzhuo Li (Ed.), Microelectronic Application of Chemical Mechanical Planarization, ISBN978-0-471-71919-9, (2008).

[3] me.berkeley.edu/ME107B/cmp/CMPsp08v2.ppt

[4] M.R. Oliver (Ed.), Chemical-Mechanical Planarization of Semiconductor Materials, Springer series in materials science, Vol. 69, 2004, ISBN 3-540-43181-0.

[5] P.B. Zantye, A. Kumar, A.K. Sikdar, Materials Science and Engineering R, Vol. 45, (2004).

[6] Gordon E. Moore, Electronics, Vol. 39, Number 8, April 19, 1965.

[7] http://www.stealth.com/faq_technology.htm

[8] http://www.intel.com/content/www/us/en/silicon-innovations/moores-law-technology.html

[9] Dan Woodie, CMP Primer, Cornel NanoScale Facility, 2007.

[10] www.erc.arizona.edu/.../CMP%20Module/CMP%20Tutorial.ppt

[11] NEXUS Market Analysis for MEMS and Microsystems III; 2005-2009.

[12] S.J. Pearton, Processing of Wide Band Gap Semiconductors, Burlington, Elsevier Science, (2000), ISBN 978-0-8155-1439-8.

[13] http://www.psma.com/sites/default/files/uploads/tech-forums-nanotechnology/presentations/2012-apec-242-ultra-rapid-nanoparticle-based-chemical-mechanical-polishing-silicon-substrates.pdf

[14] http://www.fontys.nl/fheng/werktuigbouwkunde/medewerker/gbeukema/vacuum/vacprent/cvd /cvd.html

[15] K.E. Spear, J.P. Dismukes, Synthetic Diamond: Emerging CVD Science and Technology, John Wiley and Sons Inc., (1993), ISBN 0-471-53589-3.

[16] A.G. Thornton, J. Wilks, Diamond Res. (1974), (Incl. Diamond Rev. Suppl.)

[17] A.M. Ozkan, A.P. Malshe, W.D. Brown, Diamond and Related Materials 6 (1997)1789-1798.

[18] C.Y. Wang, F.L. Zhang, T.C. Kuang, C.L. Chen, Thin Solid Films 496 (2006) 698-702.

[19] C.J. Tang, A.J. Neves, A.J.S. Fernandes, J. Gracio, N. Ali, Diamond and Related Materials 12 (2003) 1411-1416.

[20] A. Hirata, H. Tokura, M. Yoshikawa, Thin Solid Films 212 (1992) 43-48.

[21] M. Hashish, D.H. Bothel, in: M.Hashish (Ed.), Proc. of 7th Am. Waterjet Conf., Seatle, U.S.A., 1993 (August 28-31), p.793.

[22] Cecil Coutinho, Subrahmanya R. Mudhivarti, Vinay K. Gupta, Ashok Kumar, Applied Surface Science 225 (2008) 3090-3096.

[23] Y. Chen, J. Lu, Z. Chen, Microelectronic Engineering 88 (2011) 200-205.

[24] http://www.iue.tuwien.ac.at/phd/hollauer/node7.html

[25] Makoto Motoyoshi, Through Silicon Via (TSV), Proceedings of the IEEE, Vol.97, No.1, January 2009.

CHAPTER 2

CMP OF CVD DIAMOND FILMS

2.1 Introduction

Microcrystalline diamond (MCD) and Nanocrystalline diamond (NCD) films have been traditionally synthesized by different chemical vapor deposition techniques (CVD) techniques as discussed in section 1.4.1. The CVD technology has evolved over the last few decades and the process for producing high quality MCD/NCD films has been established in terms of large area deposition, grain size, and thickness of the film. In spite of numerous extraordinary properties of MCD/NCD films, it has still not found its place as in fully commercialized products. The major drawbacks of MCD/NCD films are their higher surface roughness after the CVD process. The surface roughness tends to increase as the thickness of MCD/NCD films increase [1].

With the advent of advanced CVD techniques for growing ultrananocrystalline diamond (UNCD), the surface roughness of 10-20 nm can be achieved. UNCD film, with a roughness in the range of 10-20 nm, contains graphitic (sp^2) phase at grain boundaries which significantly alters their hardness, optical transmission, and thermal conductivity. These disadvantages prohibit the use of UNCD film to its full potential in those commercialized products where extreme properties of diamond are desired [2].

In order to make MCD and NCD films useful in applications such as heat spreader in electronic packaging [3], microelectromechanical sensor for pressure and acceleration sensing [4-5], field emitter as a source of electrons [6], the surface roughness

of the CVD diamond films must be reduced by polishing techniques. Polishing can improve the performance of MCD films in following ways [1]:

- Reduces scattering of incident light, thus, improving optical transmission
- Lowers the thermal resistance
- Lowers co-efficient of friction
- Improves performance of electronic devices

In this study, diamond films are being synthesized by chemical vapor deposition technique which is described in the following section.

2.2 Synthesis of CVD Diamond Films

One of the major issues in the diamond deposition is the choice of substrate material. Diamond can be deposited onto a variety of substrate but in order to achieve good adhesion at the interface, the substrate material has to meet certain stringent requirements. These properties are non-reactive toward atomic hydrogen, stable at high temperature, low vapor pressure during deposition process, and limited solubility for carbon. Silicon stands out as an excellent non-diamond substrate material for diamond growth [7]. Therefore, in this research work Si (100) as a substrate for diamond deposition using hot-filament chemical vapor deposition (HFCVD) technique.

Prior to diamond deposition, the Si substrate is placed in a beaker with a mixture consisting of diamond particles and titanium particles in methanol. The beaker was sonicated for 20 minutes, and substrate was cleaned by purging argon gas followed by another sonication for 20 minutes. Once sonication is completed, silicon was cleaned

with methanol and purging by argon gas. The purpose of the seeding process is to incorporate surface defect sites and nucleation 'seed' for diamond growth [7].

Diamond film is deposited on the substrate, silicon in our case, from the gaseous mixture of methane and hydrogen at elevated temperature and low pressure. The gases are activated by high energy gained from hot tungsten filament clamped over the substrate as diagrammed in figure 2.1. Due to the high amount of energy supplied by the hot tungsten filament, hydrogen gets dissociated into atomic hydrogen while methane reacts to tungsten filament in order to affect its structure. The reaction between methane and tungsten filament is a process, called carburization, which alters filament structure and impacts nucleation process of diamond film [7].

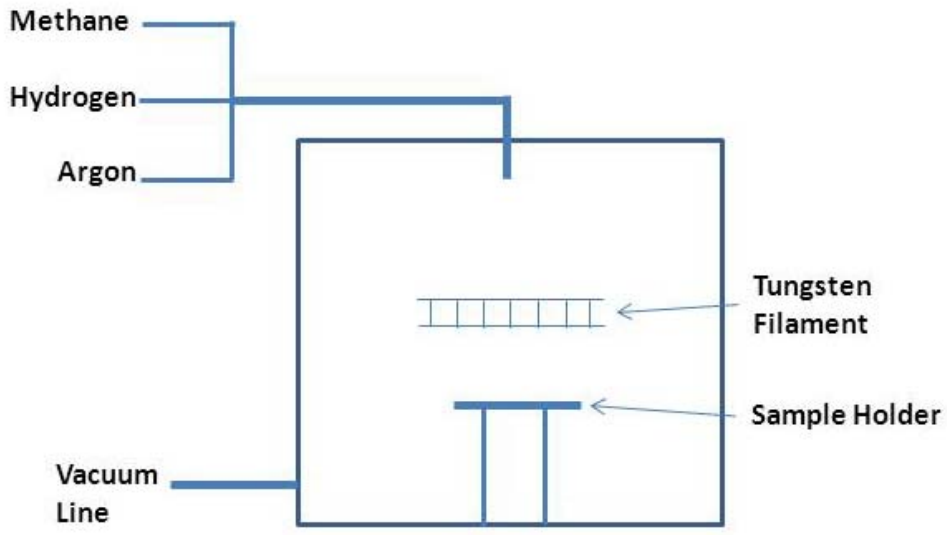

Figure 2.1 A schematic of HFCVD process

The filament, usually tungsten or tantalum, is used due to its high melting temperature during the CVD process. It requires ~1800 ^{0}C to decompose molecular hydrogen into atomic hydrogen which makes it necessary for the filament to have attained the temperature of 2500 ^{0}C. The tungsten and tantalum have melting point of

3400 ^{0}C and 3000 ^{0}C respectively, and that makes them quite suitable for use as filament. Heat transfer from the filament to the substrate is caused by radiation mode and gas phase convention mechanism and this process is known as a cold flow process because hot gases pass through hot filament and get deposited on relatively cooler substrate. In addition, substrate temperature can be manipulated by changing the distance between the filament and the substrate. For high substrate temperature, the filament is placed in close proximity to the substrate, while for low substrate temperature the filament is placed relatively far from the substrate.

Figure 2.2 The HFCVD reactor at USF

The microcrystalline diamond films were grown using the Bluewave Semiconductor® HFCVD reactor, as shown in figure 2.2, on silicon wafer. This reactor has three main components to it, namely, vacuum chamber, a roughening pump and control units for controlling temperature, pressure and flow of gasses. Cold water is supplied during the deposition process by utilizing additional chiller to cool down the chamber walls. The growth condition is shown in table 2.1.

Table 2.1 Process parameters for the CVD diamond films deposition

Process	Methane (sccm*)	Hydrogen (sccm)	Pressure (torr)	Voltage (V)	Time (hour)
Carburization	10	90	20	70	1
Deposition	3	60	20	80	5

Standard cubic centimeter per minute (0 ^{0}C, 1atm)

The optimization of process of process parameters were carried out by analyzing the Raman spectra of MCD diamond film by searching for the standard MCD peaks at the value of 1332 cm^{-1}.

2.3 Characterization of CVD Diamond Films

The synthesized diamond films are characterized by four different characterization techniques at Nanomaterials Research Laboratory (NMRL) and Nanotechnology Research and Education Center (NREC) at University of South Florida (USF). Following section gives the overview of the techniques used and the results obtained.

2.3.1 Raman Spectroscopy

Raman Spectroscopy is an extremely useful spectroscopic technique with numerous applications in the field of science and engineering due to its capability to characterize samples in solid, liquid, and gaseous form. This technique relies on the Raman effect of light, also known as Raman scattering of light, named after scientist C.V. Raman who discovered it in 1928 [8].

When light passes through a transparent substance, then it can experience two phenomena named elastic scattering and inelastic scattering. These phenomena are not mutually exclusive. These observations are true in the case X-ray beams and electron beams as well. Elastic scattering, which is also known as Rayleigh scattering, is a process where light neither gains nor loses its energy during the interaction with the sample. This implies that the wavelength of the light does not change during the interaction. As a result of elastic scattering due to incoming photons with a frequency ν_o, the molecules get excited to the virtual energy level after absorbing photon energy. Then they soon get back to the same vibrational state and emit light with same frequency ν_o as incoming photons. On the other hand, in case of inelastic scattering, the molecules, after absorbing photons of frequency ν_o, can be scattered with either lower or higher frequency than the frequency. If the resulting frequency of the vibration is reduced to $(\nu_o - \nu_m)$ then this process is called "Stokes". And if the resulting frequency of the vibration is increased to $(\nu_o + \nu_m)$, then it is called "Anti-stokes" [8]. The scattering process is schematically diagrammed in figure 2.3 [9].

Rayleigh scattering dominates Raman scattering when photons interact with molecules. As observed, 1 in 10^7 photon undergoes the Stokes Raman scattering process,

and rest of the photons contributes to Rayleigh scattering. The amount of anti-Stokes Raman scattering is even less than that of Stokes Raman scattering. This behavior can be explained in terms of the initial number of molecules in each state, which can be calculated according to Boltzmann's distribution. There are much less atoms in the excited vibrational state and therefore there are less anti-stoke scattering. Also, these conditions are dependent on the temperature [9].

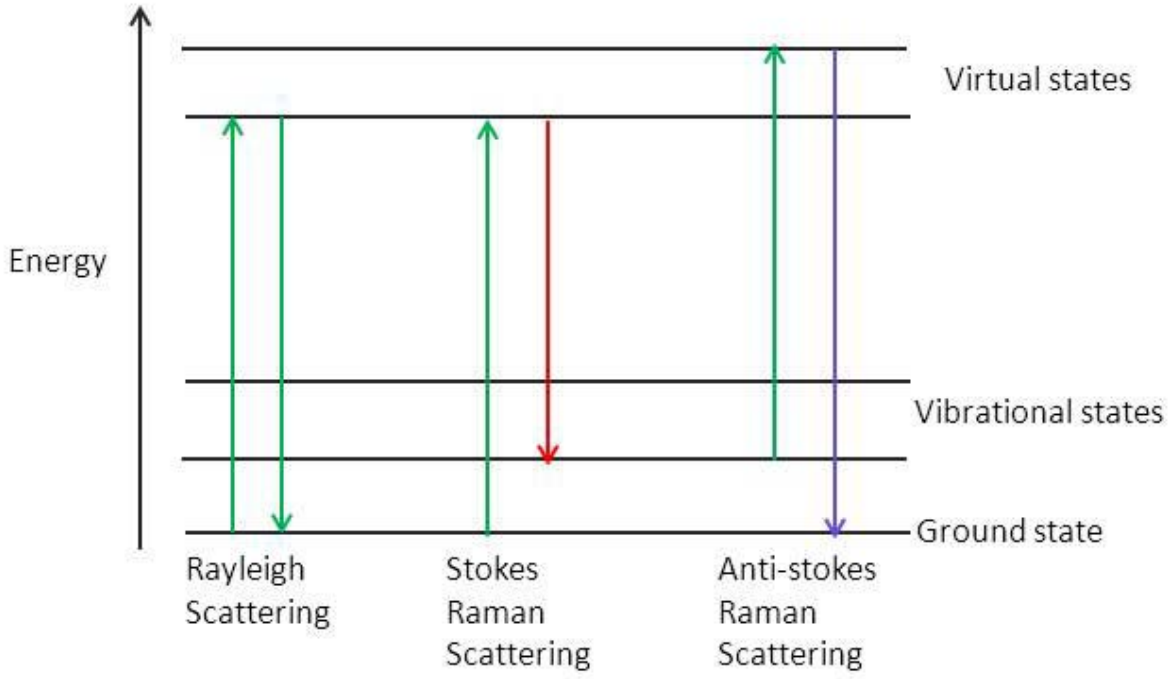

Figure 2.3 Three different forms of scattering [9]

$$N \propto exp\left(\frac{-E}{K_b T}\right) \tag{3}$$

where:

N- Number of molecules

E- Energy of the molecule

K_b- Boltzmann's constant

T-Temperature in Kelvin

The simplified working principle of Raman spectroscopy is shown in figure 2.3. A laser source having fixed wavelength (λ=514nm in the equipment at USF) is made to pass through the specimen, and in the process the phenomenon of scattering is observed by the detector. The shift in wavelength, which results from the inelastic scattering, of light can be used to gather information about the material. This information is deduced by either an analysis of the spectrum or by making comparisons with literature (fingerprinting).

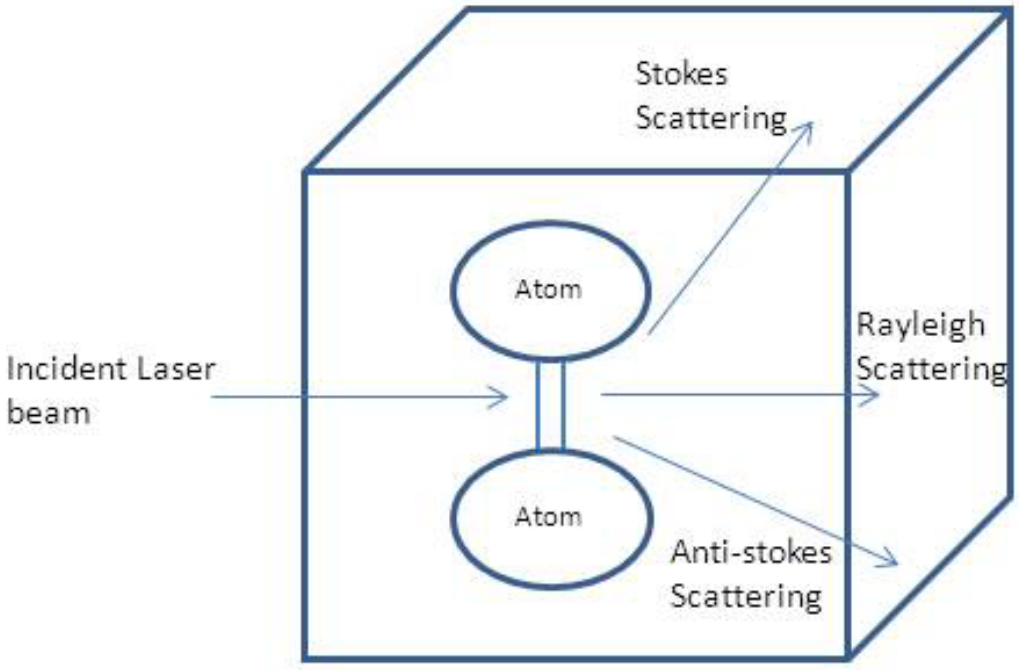

Figure 2.4 Working principle of Raman spectroscopy

The Raman spectroscopy is very sensitive to the physics and chemistry of carbon, and therefore it is used to characterize diamond films in order to get information regarding carbon bonding (sp^3/sp^2), stress state, crystallite size, and diamond to

amorphous carbon ratio. The spectral signal of the highly ordered sp^3 carbon occurs at 1332 cm^{-1}, whereas for the disordered sp^2 carbon, it is observed at 1582 cm^{-1}. The observed shift and broadening of the Raman peaks provide the aforementioned information about diamond films. However, due to the fact that sp^2 carbon (π-bonded form of carbon) has much greater Raman scattering than that of sp^3 bonded carbon, even a small percentage of sp^2 bonded carbon can sometimes provide error in quantitative analysis [10].

Figure 2.5 A photo of Raman spectroscopy system at USF

Figures 2.6, 2.7, and 2.8 show Raman spectra of CVD diamond films at three different locations in the same film: left edge, center, and right edge. The MCD peaks at

the left edge (figure 2.6), center (figure 2.7), and right edge (figure 2.8) are 1331.45 cm^{-1}, 1332.3 cm^{-1}, and 1331.45 cm^{-1} respectively. The small Raman shift from the ideal microcrystalline diamond peak of 1332 cm^{-1} represents the residual stress present the diamond film. This residual stress is caused by the difference in the thermal conductivity of diamond and silicon substrate. Since diamond cools faster than the silicon, it results in the thermal residual stress in the film. Compressive stress is considered to be induced if the peak shifts toward higher frequency, whereas tensile stress is resulted if the peak shifts toward lower frequency [11].

Stresses in the diamond film can be evaluated by models described in the literature [5-8] by using following formula:

$$\sigma = -0.567(\omega - \omega_0)\ GPa \tag{4}$$

where:

σ – Stress in the film

ω – Actual frequency at which peak is observed

ω_0 – Stress free standard peak of microcrystalline diamond considering (111) plane

Therefore, the residual stress in the synthesized diamond film at left edge, center, and right edge are 0.312 GPa (tensile), -0.3GPa (compressive), and 0.312 GPa (tensile) respectively.

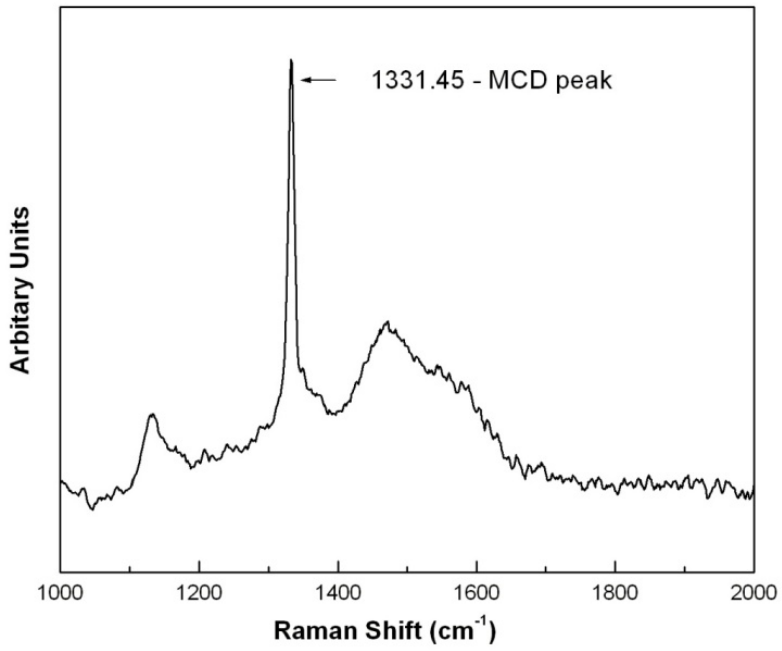

Figure 2.6 MCD spectra of CVD diamond film at the left corner

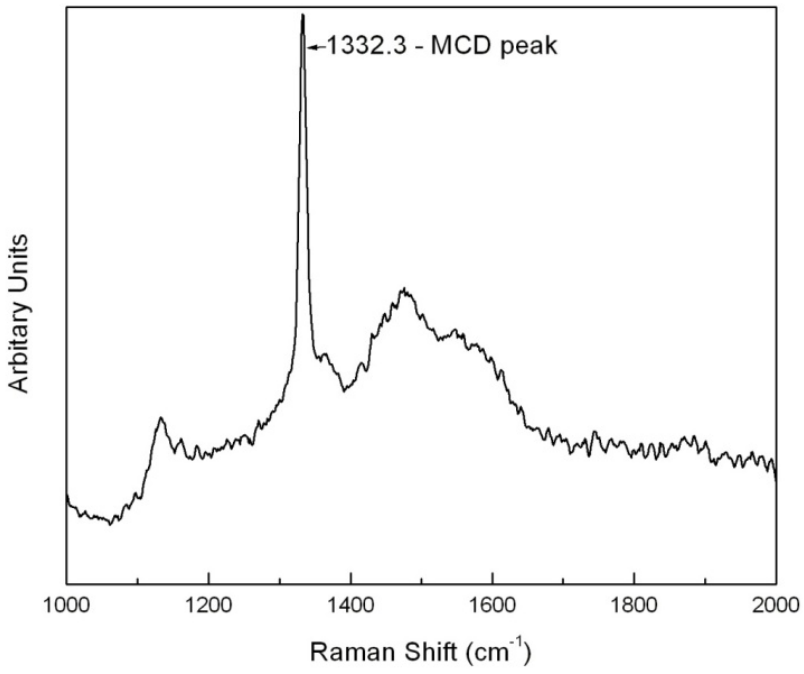

Figure 2.7 MCD spectra of CVD diamond film at the center

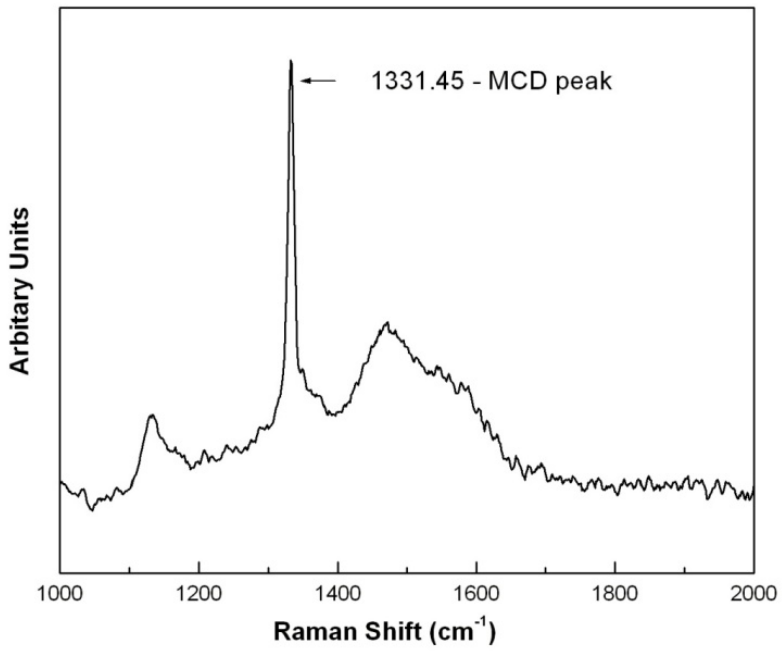

Figure 2.8 MCD spectra of CVD diamond film at the right corner

2.3.2 Atomic Force Microscopy

Atomic force microscopy, a technique capable of measuring surface topography in nanoscale, was invented by Gerd Binning and Heinrich Rohrer in the 1985 at IBM®. This technique was developed to overcome shortcomings of the Scanning Tunneling Microscopy (STM), which was not capable of imaging non-conductive samples. As a result of the development of AFM, it was possible to measure the surface topography of a variety of samples, including conducting, semiconducting, non-ducting, ceramics, polymer, and biological samples [12].

Fundamentally, AFM works on the principle of interaction between two solids at the atomic level. Here, the interaction between a sharp needle like probe and surface of sample is monitored to get topographical image of the surface of the sample. The sharp cantilever, typically made from silicon or silicon nitride (Si_3N_4), comes into close

proximity with the surface of the sample, and the deflection of the cantilever is recorded by laser and a photodetector as represented in figure 2.9 [12]. Figure 2.10 shows the graph between force and interatomic separation when the cantilever and surface of the sample are brought into close proximity to each other [12].

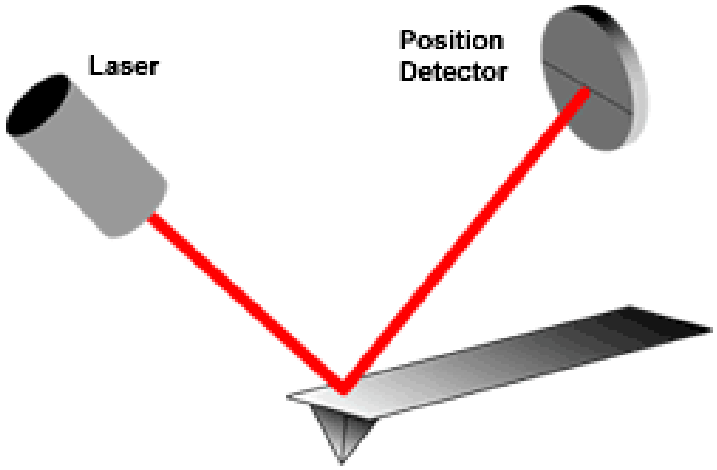

Figure 2.9 Detection of cantilever deflection by laser and photodetector [12]

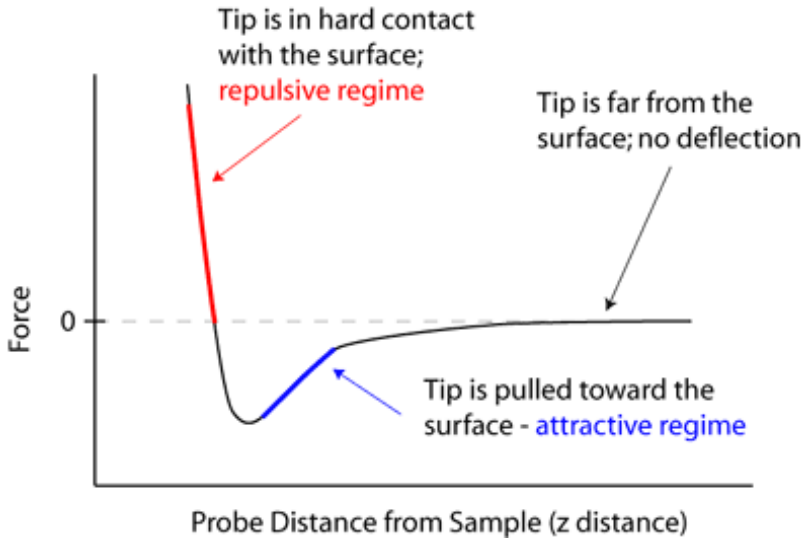

Figure 2.10 Variation of force versus the interatomic separation between atoms of sample and cantilever [12]

The topography of CVD diamond films were observed by using SPM-AFM Digital Instrument Dimension 3100® in non-contact mode. AFM images for different scanning area and different dimension are shown in figure 2.11. The average roughness was found to 37 nm for the CVD diamond films.

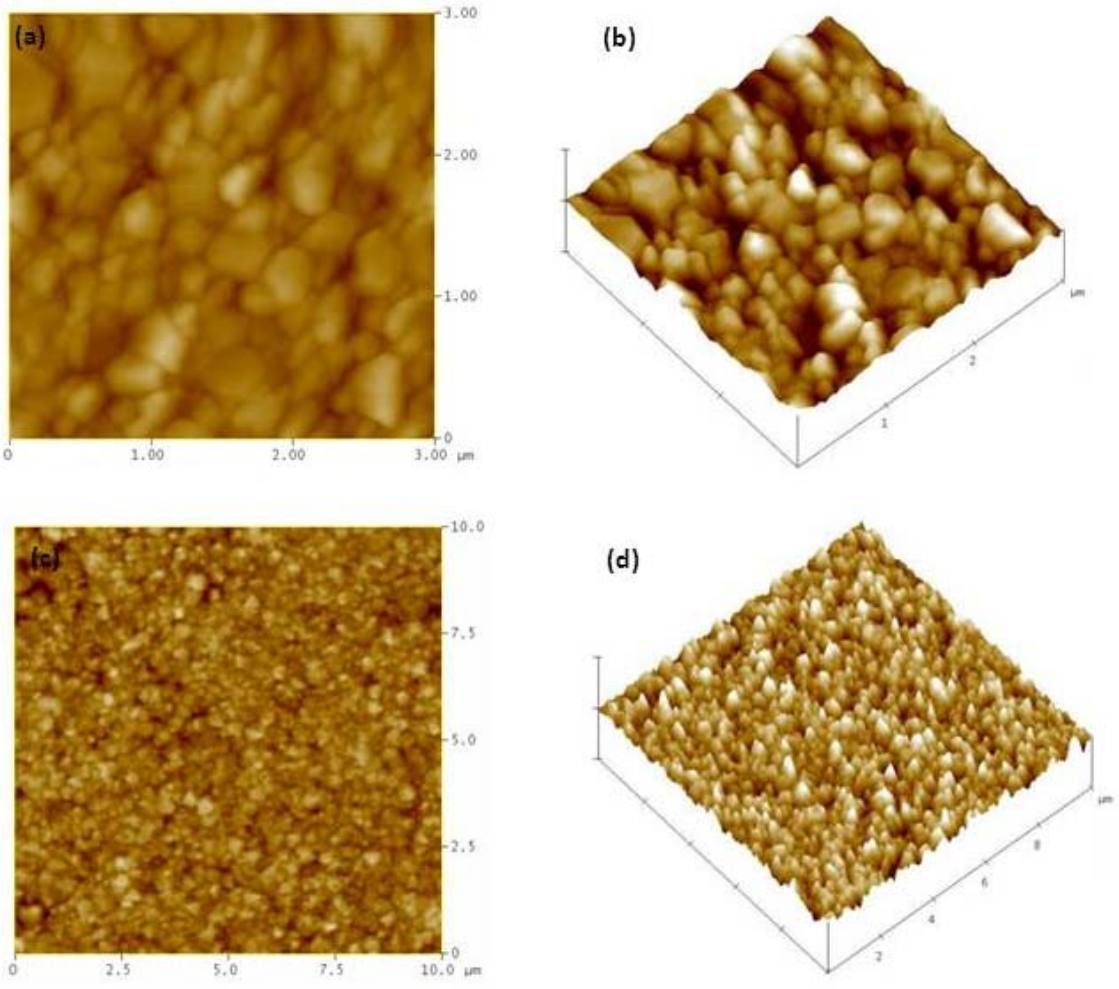

Figure 2.11 AFM scan of MCD film (a) 2D with scan area of 3 µm ×3 µm (b) 2D with scan area of 3 µm ×3 µm (c) 2D with scan area of 10 µm ×10 µm (d) 3D with scan area of 10 µm ×10 µm

2.3.3 Scanning Electron Microscopy

Scanning electron microscope (SEM) is the most versatile characterization technique used in the field of materials science, physics, chemistry, engineering and other applied sciences due to its capabilities such as excellent depth of focus, resolution etc. SEM was commercialized approximately 50 years ago and since then it has evolved at high pace to keep up the demands of scientific and engineering communities. Today, there are several types of SEM available in the market. Each dealing with the specific customer requirements although the each of them have the same fundamental working principle.

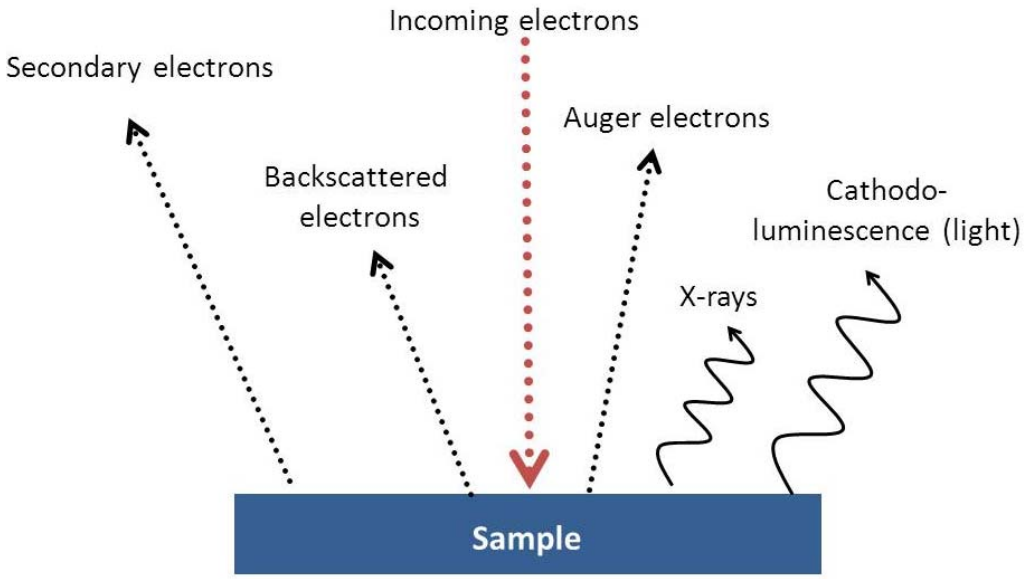

Figure 2.12 Simplified interactions between beam of electrons and sample [13]

The working principle of SEM relies on the fundamental theory of interaction between beams of electrons and the surface of a conductive sample. As a result, different types of signals including Auger's electrons, secondary electrons, backscattered electrons, X-rays, and cathodoluminescence emanate from different depth of the surface

of the sample as schematically diagrammed in figure 2.12 [13]. Secondary electrons are considered to be an important signal for SEM and are attracted by an ET detector, invented by Thomas Everhart and Richard Thornley and hence the name. ET detector consists of three major parts namely, a collector, a scintillator, and a photomultiplier. Secondary electrons coming out from the surface of the sample move toward the collector due to its high potential. The scintillator, having a high positive bias, converts secondary electrons into photons that pass through the light tube. The photomultiplier uses these photons for signal gain which is further enhanced for the screen display. A schematic of ET detector is shown in figure 2.13[14]

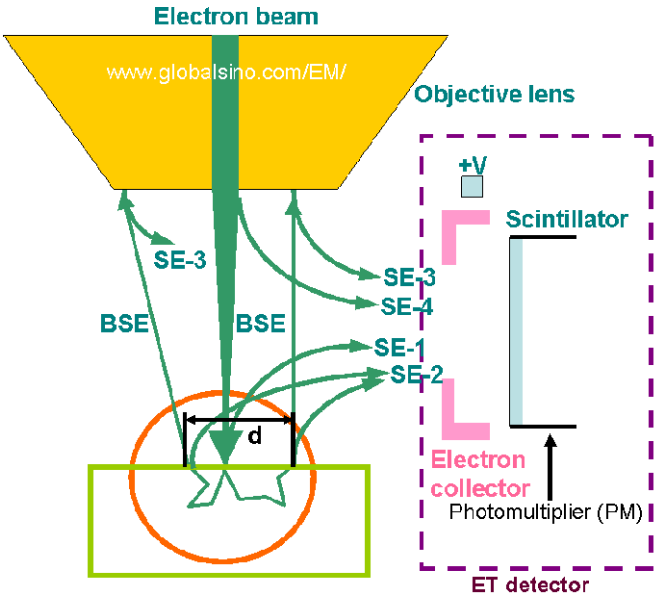

Figure 2.13 A construction of ET detector [14]

Figure 2.14 shows the SEM micrograph of CVD diamond film at different magnifications. The presence of different crystal orientations is evident from these images.

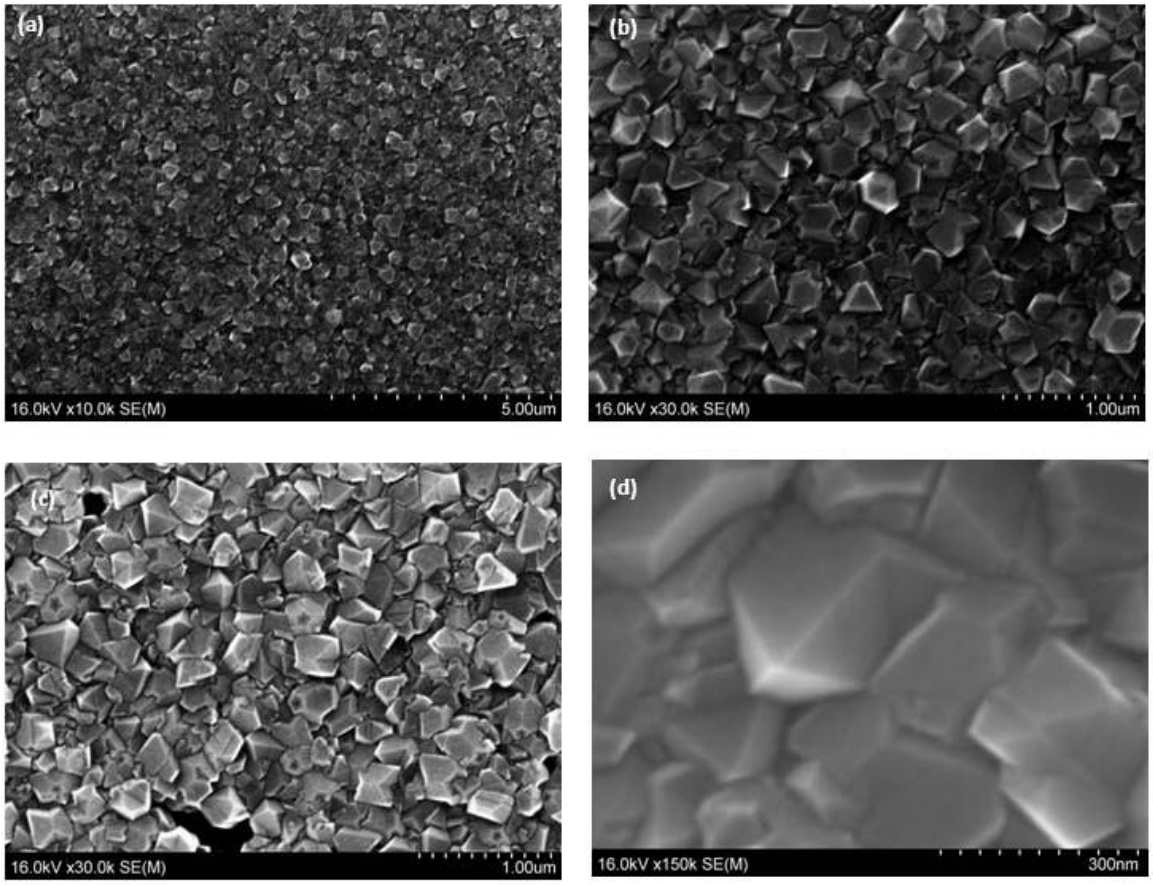

Figure 2.14 SEM micrographs of MCD diamond film at (a,b,c) 30,000X (d) 150,000X.

2.3.4 X-ray Diffractions

X-rays were discovered by physicist Wilhelm Rőntgen, and are electromagnetic radiations which have wavelengths in the range of 0.1 to 100 Å. Its wavelength lies between the Gamma rays and Ultraviolet rays on the electromagnetic spectrum. X-ray diffraction by crystal and its application to determine crystal structure were invented by Max von Laue in 1912 and W.L. Bragg and W.H. Bragg in between 1912-1920 respectively. Since then, this technique has been utilized to determine crystal structure of nearly all crystalline materials.

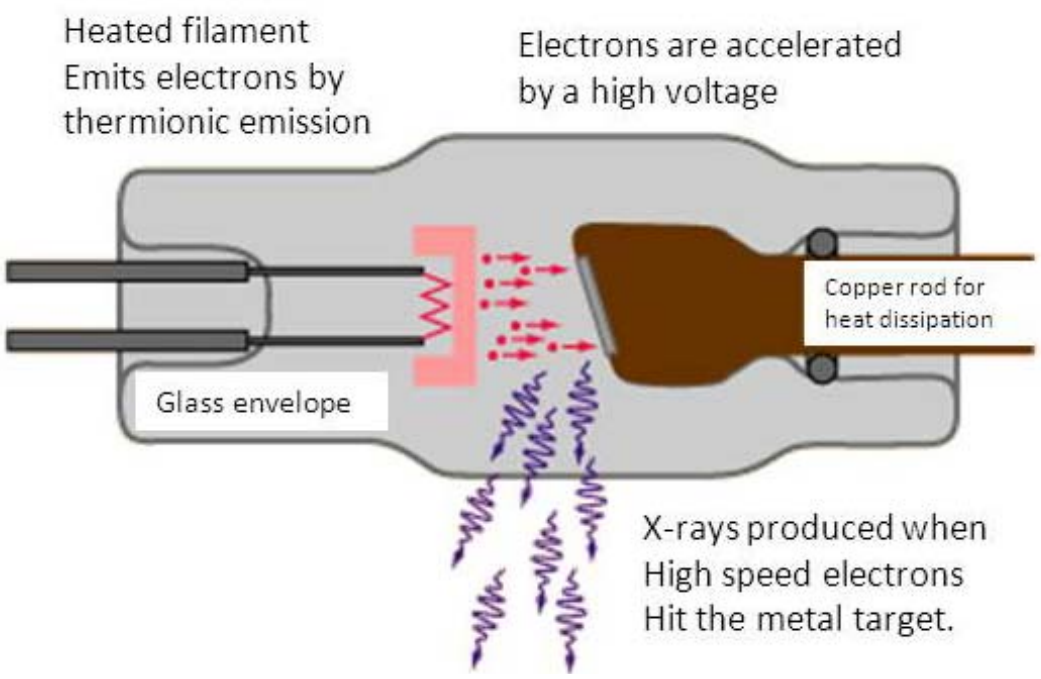

Figure 2.15 A schematic of X-ray production [15]

To carry out X-ray diffraction (XRD) by crystal of a material, X-rays are produced by a metal target and an electron source that are placed in the vacuum-sealed tube acting as an anode and a cathode respectively. This is schematically shown in figure 2.16 [15]. Electrons are ejected by a heated metal which acts as an electron source, and these electrons hit the surface of the water-cooled metal target and as a result, produce X-rays. During the interaction of electron upon the metal target, electrons lose most of their kinetic energy as heat dissipation and a very small percentage (~1%) is converted into X-rays. These resultant X-rays are then subjected to diffraction by crystalline material, and this phenomena is governed by Bragg's Law of diffraction:

$$n\lambda = 2d \sin\theta \tag{5}$$

where:

n- Order of diffraction

λ- Wavelength of X-rays

d- Interplanar distance between crystallographic planes

θ- Angle of diffraction

The XRD spectra of MCD film is shown in figure 2.17. The y-axis represents the scattering intensity while the X-axis represents the scattering angle 2θ. Different crystallographic planes of a crystalline material can be observed in XRD spectra by varying the angle of X-ray incidence on the sample surface. These XRD spectra were matched by the standard data using the HighScore Datebase® and literature search.

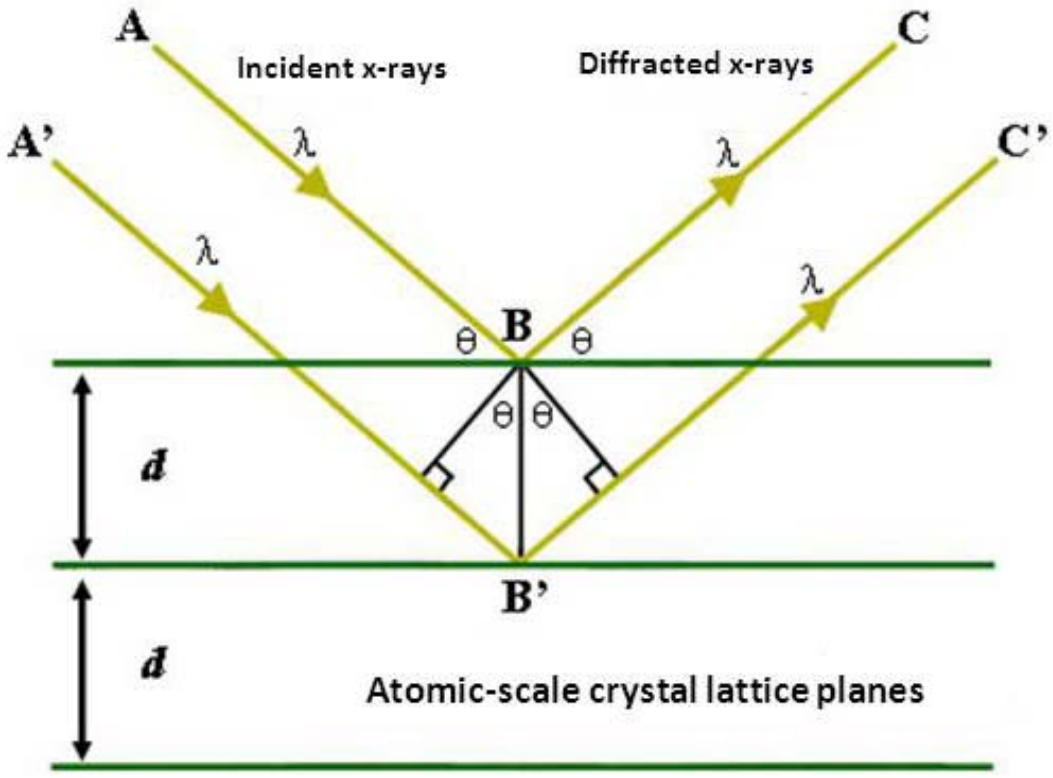

Figure 2.16 A schematic representation of Bragg's Law [16]

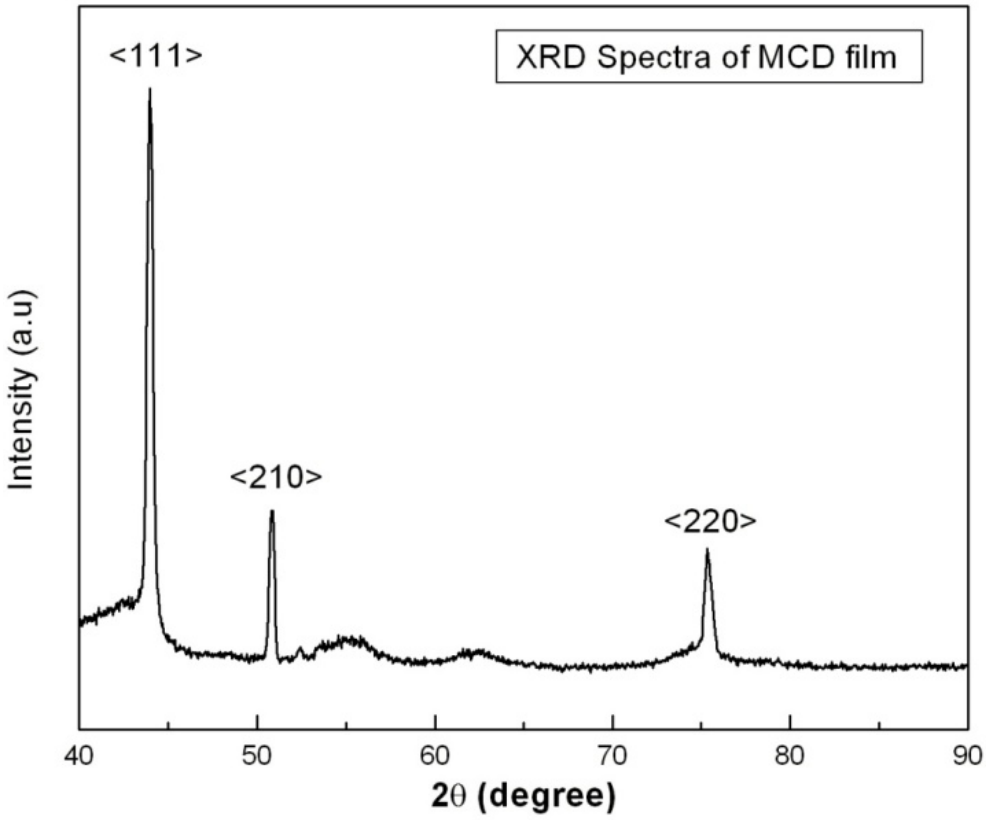

Figure 2.17 XRD spectra of MCD film

2.4 CMP of CVD Diamond Films

The CETR CP-4 bench-top CMP tester, as shown in figure 2.18, is used for the polishing of CVD diamond wafers. The universal material tester (UMT) at USF is capable of performing a variety of tribological tests, including:

- Pin on disc
- Ball on disc
- Ball on one, two or three balls
- Pin on V-block
- Block on ring
- Disc on disc (flat on flat)

Among the above mentioned modes, disc on disc is utilized for carrying out CMP of a wafer. The CMP tester is equipped with dual force sensors which can measure forces in X (lateral) and Y (normal) directions, thus, providing a real time coefficient of friction during the polishing process. The wafer is mounted upside down between retaining rings to keep it horizontally aligned. The carrier stage has 2D dual force sensors, lateral positioning system, and a mechanism to provide constant pressure while pressing wafer against the polishing pad. The circular polishing pad is made to stick with a horizontal rotational drive motor capable of providing desired torque and speed during polishing [17]. The slurry, typically a mixture of abrasive particles and chemical additives, is made to flow on the center of the pad which due the action of centrifugal force gets uniformly distributed on the entire pad surface. This helps creating a thin fluid layer across the pad surface.

The two components mechanical and chemical occur simultaneously during CMP process and are considered to be inseparable. The mechanical action is described by the controlled speed and pressure, and that subsequently causes two-body abrasion between either abrasive and wafer or abrasive and pad. The interaction between pad, abrasive and wafers are considered to be a three body abrasion system. On the other hand, chemical action is described by the reaction occurring between chemical reagents in slurry and wafer, which in turn results in the modification of wafer surface enhancing its removal. The chemical reagents are tailored toward a particular wafer and its characteristics to react in way that helps efficient material removal. Wafers or thin films have their own properties and chemical additives in the slurry must be designed

accordingly. Besides, chemical additives assist in dissolving the abraded materials and preventing them from re-deposition onto the wafer surface [18].

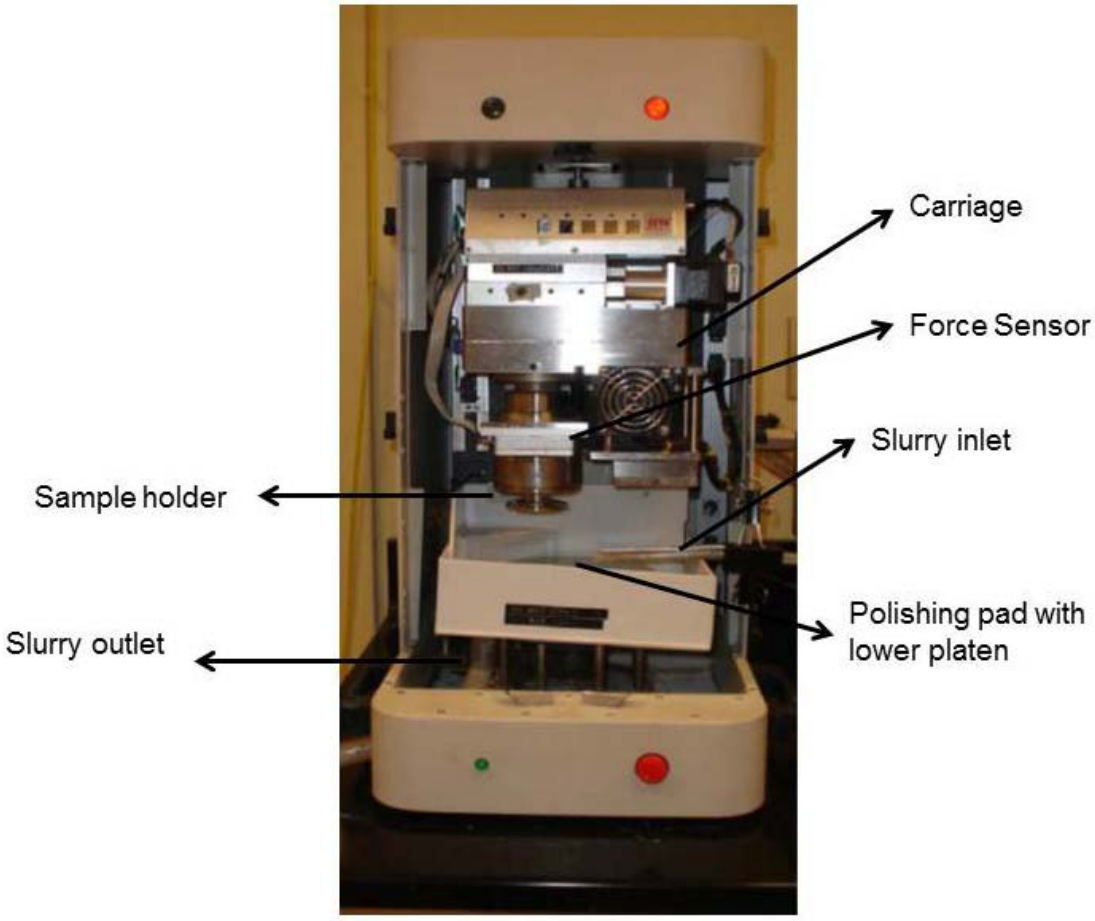

Figure 2.18 A CMP bench top tester

The CVD diamond wafer of size 20 cm X 20cm was used for polishing. Prior to the polishing, the polishing pad is subjected to the conditioning process for 10 minutes using de-ionized water and diamond conditioner from 3M with a grit size of 400. The purpose of the conditioning process is to keep required asperity structure of the pad surface and to maintain a uniform removal rate during the CMP process. This also helps in the uniform distribution of the slurry and the removal of by-products during polishing.

Before actual polishing, the wafer was cleaned by an acetone solution and by purging compressed nitrogen gas in order to remove surface contaminants. The CVD diamond wafer was attached to the sample holder, which is capable of holding a sample up to the size of a 4 cm X 4 cm wafer. The polishing was done for 60 seconds.

The polishing of CVD diamond films were carried out using the standard slurry procured from Logitech Inc. UK. Polishing was first performed using the boron carbide powder (0.5%, 1.0%, and 1.5% solution in de-ionized water) which is followed by finish polishing by calcinated aluminum oxide powder (1% solution in de-ionized water) in order to achieve higher degree of planarity.

The material removal rate for diamond films was calculated by using following formula:

$$MRR = \frac{M_i - M_f}{\rho \times A \times t} \tag{6}$$

where:

M_i – Mass of the diamond film before polishing

M_f – Mass of diamond film after polishing

ρ – Density of diamond

A – Area of wafer

t – Time of polishing

The thickness of the diamond films were calculated by using a micrometer at Nanotechnology Research and Education Center (NREC), USF. The thickness was measured at five places including, each corner and center. The average value was taken for the calculation of the material removal rate.

2.5 Results and Discussion

2.5.1 Polishing Parameters

The planarization of CVD diamond (microcrystalline and nanocrystalline) films were performed on CMP bench-top tester as described in section 2.4. Polishing parameters were optimized for maximum removal rate and are shown in table 2.2. The optimizations of polishing parameters were done by utilizing dummy MCD films and DI water.

Table 2.2 Polishing parameters for CVD diamond CMP process

Process Parameters	Value
Pressure	3 psi
Relative speed	100 rpm
Slurry	Boron Carbide (0.5, 1.0, 1.5 wt.%)+de-ionized (DI) water
Time	60 Seconds
Pad	Suba IV/IC 1000
Slurry flow rate	60 ml/min

2.5.2 CMP Performance

The slurry composition is varied in terms of abrasive content by varying the percentage of boron carbide in the slurry. The material removal rate increases by increasing the percentage of boron carbide content in the slurry. Figure 2.19 shows the graphical representation of material removal variation.

The surface roughness of the MCD and NCD films were analyzed by using atomic force microscopy (AFM). The surface roughness of MCD films were reduced from 37nm to 15nm by CMP polishing as shown in figure 2.20. The reduction in roughness is attributed to the abrasive action by hard boron carbide particles. There are

few scratches present in the polished surface which is plausibly caused by agglomerated boron carbide particles during the polishing of MCD films.

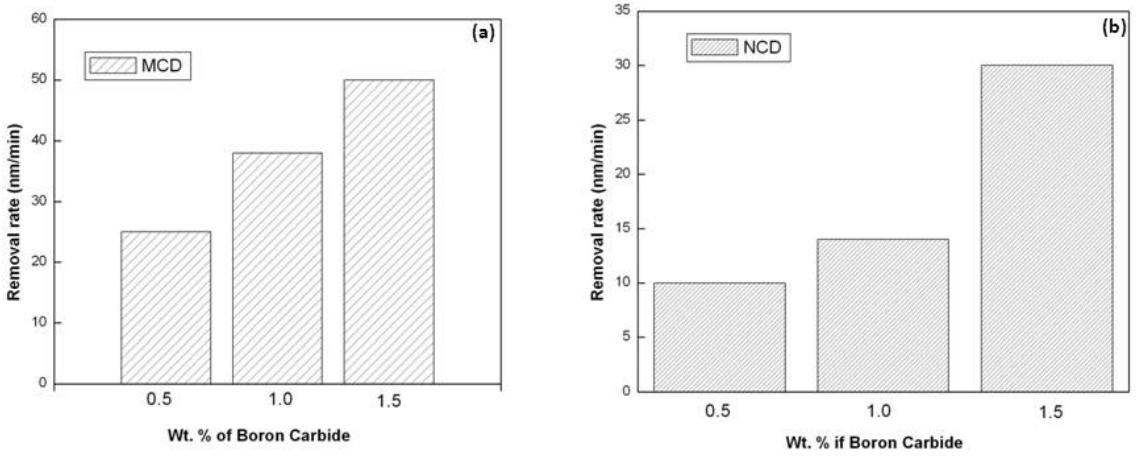

Figure 2.19 Material removal rates versus abrasive content for (a) MCD (b) NCD

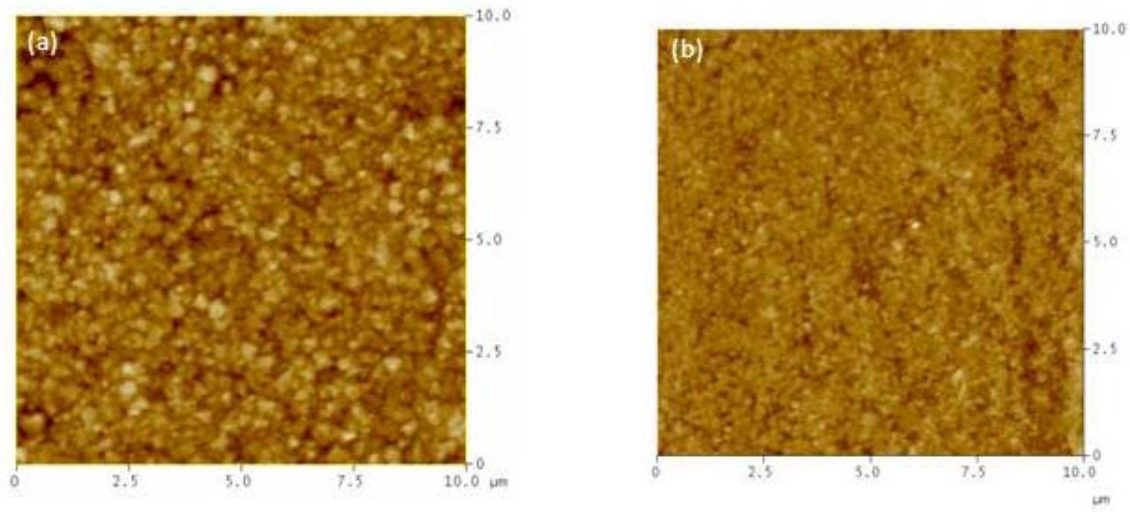

Figure 2.20 AFM surface scan (a) before CMP (b) after CMP of MCD film

The surface roughness value for NCD diamond film showed less material removal rate in comparison with MCD diamond film. The surface roughness of NCD

films were reduced from 18nm to 12 nm by polishing for 60 seconds. The AFM surface scans are shown in figure 2.21.

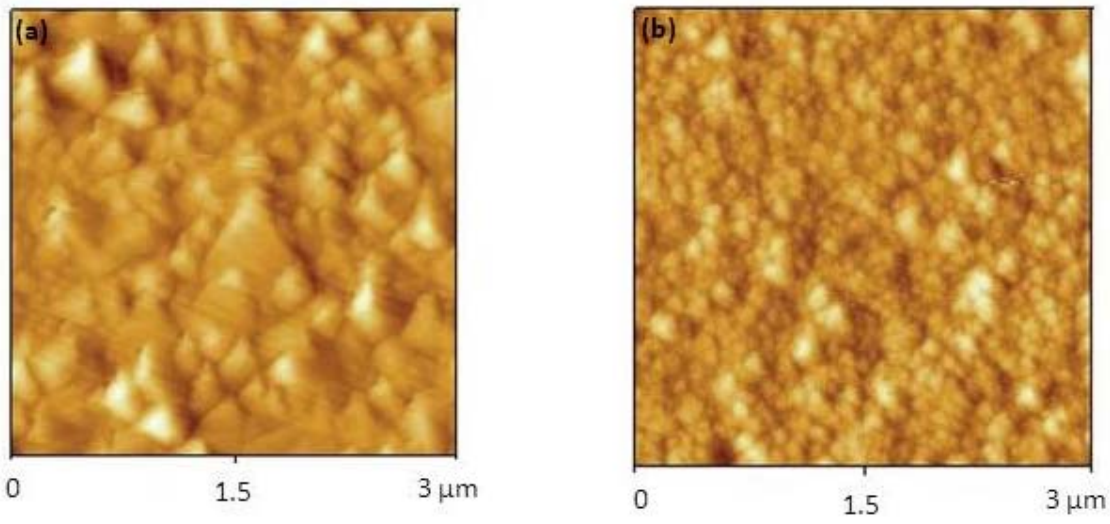

Figure 2.21 AFM surface (a) before CMP (b) after CMP of NCD film

The plausible mechanism for the material removal from diamond films can be explained on the basis of breaking of carbon-carbon bonds at the surface of diamond films. The small indentation produced by the interaction between abrasive particles and the diamond surface causes the weakening of the C-C bonds, which leads to the dissolution of the surface of diamond films. Alternatively this process can be explained in terms of micro-chipping, fracture, and abrasion of diamond films by the abrasive particles [1].The polishing pressure was kept low at 3 psi in order to avoid change in the sp^3 form of carbon into sp^2 carbon [19].

2.6 Summary

In this part of the thesis, the CVD diamond films have been synthesized by optimizing process parameters in the HFCVD reaction chamber. The optimum process parameters produced high quality diamond films as evident by characterization results obtained from Raman Spectroscopy, SEM, AFM, and XRD. The CVD diamond films, both MCD and NCD, were polished using CETR bench-top CMP tester by using commercial slurry. The post-CMP average surface roughness analysis of the MCD and NCD diamond films were carried out using AFM and the significant reduction in the surface roughness was observed. The material removal rates were calculated for the polishing by varying content of the abrasive in the slurry. The material removal from diamond films were possibly caused by the abrasion, micro-chipping, and micro-fracture by the boron carbide particles in the slurry.

2.7 References

[1] C.J. Tang, A.J. Neves, A.J.S. Fernandes, J. Gracio, N. Ali, Diamond and Related Materials 12 (2003) 1411-1416.

[2] A. Chakkaravarthi, R.K. Singh, D. Singh, MRS 2010 Spring Meeting, Symposium E: Chemical Mechanical Planarization as a Semiconductor Technology Enabler.

[3] K. Jagannadham, Solid-State Electronics, 42 (1998) 2199-2208.

[4] E. Kohn, P. Gluche, M. Adamschik, Diamond and Related Materials 8 (1999) 934-940.

[5] N. Sepulveda, D. Aslam, J.P. Sullivan, Diamond and Related Materials 15 (2006) 398-403.

[6] Satyaharish Jeedigunta, Ph.D., Dissertation, University of South Florida, 2008.

[7] S.J. Pearton, Processing of Wide Band Gap Semiconductors, Burlington, Elsevier Science, (2000).

[8] E. Smith, G. Dent, Modern Raman Spectroscopy: A practical Approach, John Wiley & Sons Inc., June (2005), eISBN 9780470011829.

[9] http://www.doitpoms.ac.uk/tlplib/raman/printall.php

[10] Irfan Ahmad, M.S., Thesis, University of Alabama, (1997)

[11] G. Turrell and J. Corset, Raman Microscopy: development and application, 1st edition, Academic Press Inc., ISBN 0-12-189690-0, (1996).

[12] http://www.nanoscience.com/education/afm.html

[13] www.uio.no/studier/emner/matnat/fys/.../v09/.../24february09.ppt

[14] http://www.globalsino.com/EM/page4584.html

[15] http://hyperphysics.phy-astr.gsu.edu/hbase/quantum/xtube.html

[16] http://serc.carleton.edu/research_education/geochemsheets/BraggsLaw.html

[17] CETR UMT Hardware Installation & Application Manual, Center For Triblogy, Campbell, CA 95008.

[18] Parshuram B. Zantye, Ashok Kumar, A.K. Sikdar, 'Materials Science and Engineering R, Vol. 45 pp. 89-220 (2004).

[19] C.Y. Wang, F.L. Zhang, T.C. Kuang, C.L. Chen, Thin Solid Films 496 (2006) 698-702.

CHAPTER 3

CMP OF SILICON DIOXIDE

3.1 Introduction

The silicon dioxide CMP process has become very important in the present state-of-the-art semiconductor industries due to the advent of new technologies like shallow trench isolation. This led to the high demands in terms of planarization efficiency, removal rate, surface scratches, within wafer nonuniformity, and wafer-to-wafer nonuniformity. As the device feature sizes have been shrinking, the requirements of surface planarization become stringent during the manufacturing of integrated circuits (IC). To incorporate and accommodate the improvements such as decreased feature size, increased device speed and more intricate designs, research in the 'back end of the line' (BEOL) processes has become equally important as the development of the 'front end of line' (FEOL) processes to reduce gate oxide thickness and channel length. Chemical mechanical planarization is the key process in manufacturing of semiconductor devices due to its excellent ability for global planarization of multilevel interconnects and at same time leading to low cost of ownership [1]. In CMP process materials are removed by polishing the "hills" on the wafer and "flattening" the thin film. Usually, in the electronic manufacturing industry a wafer has to go through approximately 15 CMP steps [2]. Hence it is of utmost importance to optimize CMP process parameters which leads towards high efficiency and low cost of ownership.

In the past decades, nanodiamond (NDs) particles have gained worldwide attention due to their inexpensive large scale synthesis with narrow size (4-5 nm) distribution. These nanodiamond particles possess non-toxicity, facile surface functionalization, biocompatibility, quantum information processing, magnetotometry, novel imaging, and infra-red (IR) fluorescence [3]. Due to aforementioned exceptional properties of nanodiamond particles, it opens door for many novel applications. Under this research work, the exceptional abrasive and environmentally benign properties of nanodiamond particles in the synthesis of CMP slurry for oxide polishing. In this investigation, composite particles containing nanodiamond dispersed within cross-linked, polymeric microspheres were developed. And the CMP of thermal oxide layer has been analyzed using conventional ceria particles based slurry and synthesized novel nanodiamond-polymer based slurry.

3.2 Synthesis of Silicon Dioxide Films

The silicon dioxide films, commonly known as oxide, were procured from Sematech International. The oxide films were grown in plasma-enhanced chemical vapor deposition (PECVD) system. The precursor gasses used were SiH_4 (silane), N_2O (Nitrous oxide), and N_2 (Nitrogen). The substrate temperature was maintained at 400^0C during the deposition process. As a result, the oxide film of thickness 3850 nm was obtained [4].

3.3 CMP Slurry Development

3.3.1 Synthesis of CMP Slurry

Unless otherwise mentioned, all the chemicals were purchased from Sigma-Aldrich and used without further purification. Chemicals used were N-isopropylacrylamide (NIPAM), N,N'-methylenebisacrylamide, 3-(trimethoxysilyl) propyl methacrylate (MPS), Sodium salt of poly(acrylic acid) (PAAc), potassium persulfate, sodium hydroxide (NaOH), hydrochloric acid (HCl) and nanodiamond powder. Nanodiamond powders were procured from International Nanotechnology Center (ITC, Raleigh, NC).

Polymerization of NIPAM (5g) were carried out in the aqueous solution (1000ml) by using cross linking material N,N'-methylenebisacrylamide (0.2g) and the reaction mixture was purged using nitrogen for 1 hour. After that, an ionic initiator potassium persulfate (0.1g) was added to the reaction mixture and it was heated to 75 degree in an oil bath. After 2 hours, MPS was added as a co-monomer and the polymerization was continued to 1 hour more. Interpenetration chains of poly (acrylic acid) were introduced by adding the sodium salt of PAAc (~10g, Molecular weight ~ 15,000 g/mole) into the reaction mixture. The resulting material after the addition of interpenetrating chains of PAAc is called as IP-Hybrid Microcomposites. The prepared IP-hybrid was purified by repeated centrifugation using Labnet Hermle Z200A.

To make nanodiamond-polymer composite particle, nanodiamond particles suspended in deionized water were mixed with prepared IP-hybrid at 40 degree. The pH of the solution was maintained at 5 by using 0.1 M NaOH and 0.1 M HCl. The resultant mixture was settled at the bottom and the supernatant was removed. The removed

composites were re-dispersed in deionized water and put in the magnetic stirrer for 1 minute. The synthesized particles were allowed to naturally sediment for 30 minutes and then it supernatant was removed and dispersed in deionized water. This process was repeated three times and the supernatant was collected to be used as slurry with desired dilution. In addition, the conventional ceria based slurry is also used for oxide polishing. The ceria nanoparticles were mixed with de-ionized water in order to make ceria-based slurry.

3.3.2 Characterization of CMP Slurry

Transmission electron microscopy (TEM) was used to characterize the synthesized novel nanodiamond polymer slurry, and conventional ceria based slurry. The main purpose of this characterization was to investigate the dispersion of diamond particles in the polymer matrix in case of novel nanodiamond polymer based slurry, and dispersion of ceria nanoparticles in the ceria-DI slurry. Figure 3.1 and 3.2 show TEM images of the ceria nanoparticles and the synthesized slurry respectively.

From the TEM images of the ceria nanoparticles, it can be clearly seen that the ceria nanoparticles are uniformly distributed without large amount of agglomeration. In case of nanodiamond-polymer slurry, the nanodiamond particle is attached to the polymer matrix continuously throughout the matrix. This gives cushioning effect by soft polymer matrix during the polishing.

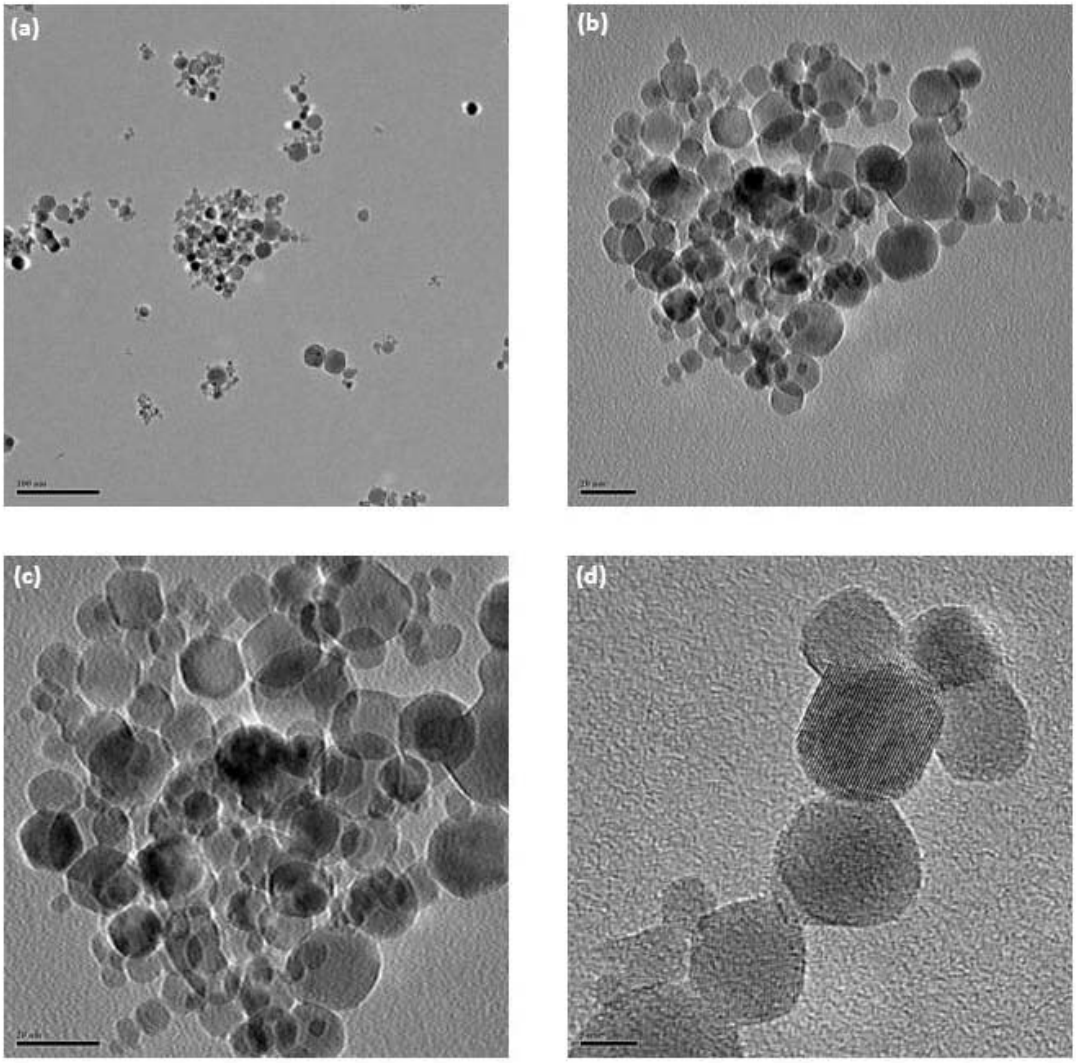

Figure 3.1 TEM image of ceria nanoparticle at different magnifications

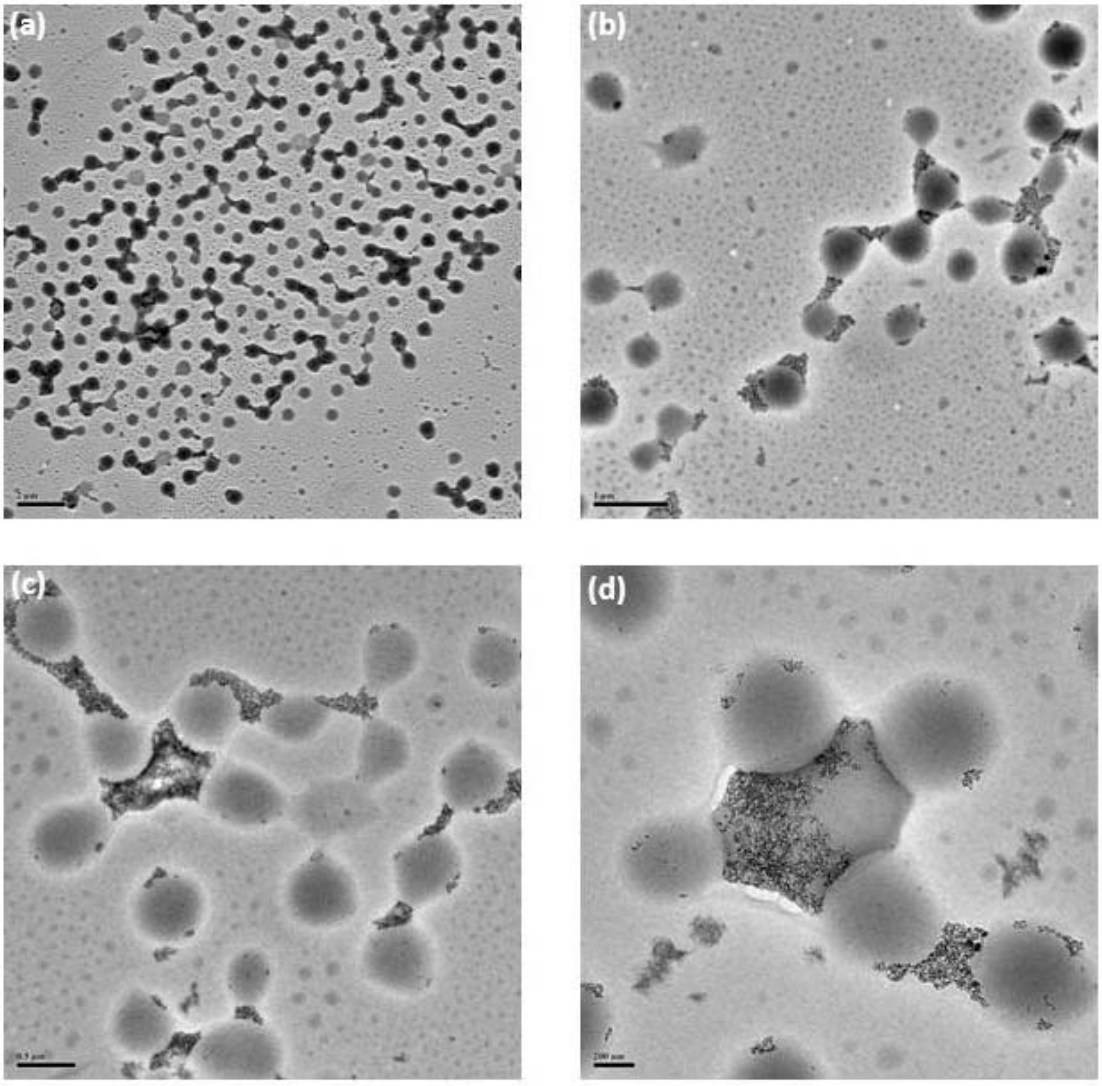

Figure 3.2 TEM images of nanodiamond-polymer based slurry at different magnification

3.4 CMP of Silicon Dioxide Films

The CMP of silicon dioxide was performed in CETR bench-top CMP tester, and the similar procedure as described in section 2.3. The pad used in the polishing processes was Suba IV, and its properties are shown in table 3.1. Prior to the polishing of oxide films, polishing pad was conditioned for 20 minutes using deionized water in the place of the slurry. The main purpose of the conditioning was to keep the pad properties

uniform during polishing process. The polishing pad was replaced after 20 polishing cycles of the wafer.

Table 3.1 Properties of IC 1000/Suba IV pads

Polishing Pad properties	Value
Hardness	57 (Shore D)
Compressibility	2.25%
Thickness	1.275 mm
Specific gravity	630-800 (kg/cm^3)
Diameter	81 cm

The polishing of oxide wafers were done by utilizing conventional ceria based slurry as well as synthesized nanodiamond-polymer based slurry. The weight percentages of slurries were kept at 0.5 % in deionized water. Both of the slurries were dispersed in the deionized water at a pH value of 5 during the polishing of oxide films. The CMP experiments were performed at the room temperature. The optimized process parameters used in the polishing are shown in table 3.2

Table 3.2 Polishing parameters for oxide CMP process

Process Parameters	Value
Pressure	6 psi
Relative speed	150 rpm
Slurry	Ceria (0.5 wt.%), and Novel nanodiamond-polymer based slurry (0.5 wt.%)
Time	60 Seconds
Pad	Suba IV/IC 1000
Slurry flow rate	70 ml/min

3.5 Results and Discussion

The material removal rates were calculated by the formula mentioned in the chapter 3 (Equation#6). The novel nanodiamond-polymer based slurry showed less material removal rate than the material removal obtained by ceria based slurry. This behavior can be attributed to the tooth property of ceria particles in the slurry [5].The observed material removal rate are similar to the value reported in the literature by other researcher and scientists. Cecil and coworkers showed the removal rate of 236nm/min by consuming 0.5wt.% ceria in their investigation [6]. Since no chemical additive is used in ceria based slurry, the slurry performance can be further enhanced by adding suitable chemical additives.

Table 3.3 Output parameters for oxide CMP process

Slurry	Removal rate (nm/min)	Co-efficient of friction
Nanodiamond-polymer	120 ± 1.20	0.160 ± 0.019
Ceria	192 ± 0.75	0.206 ± 0.017

The *in-situ* co-efficient of friction data were collected by the CETR software system. It utilizes the dual force sensor in order to measure the value of lateral and normal forces during the polishing process. The values of coefficient of friction presented in table 3.3 are the steady state values. The values of coefficient of friction obtained by polishing of oxide films using novel nanodiamond-polymer based slurry was less than the coefficient of friction obtained by using ceria based slurry. This behavior can be attributed to the fact that polymer matrix presence in the slurry during polishing by novel nanodiamond-polymer based slurry provided softness during the polishing. This phenomenon is commonly known as cushioning effect provided by the soft polymer

matrix during the polishing of oxide films. Table 3.3 shows the values of removal rate and coefficient of friction obtained by both slurries.

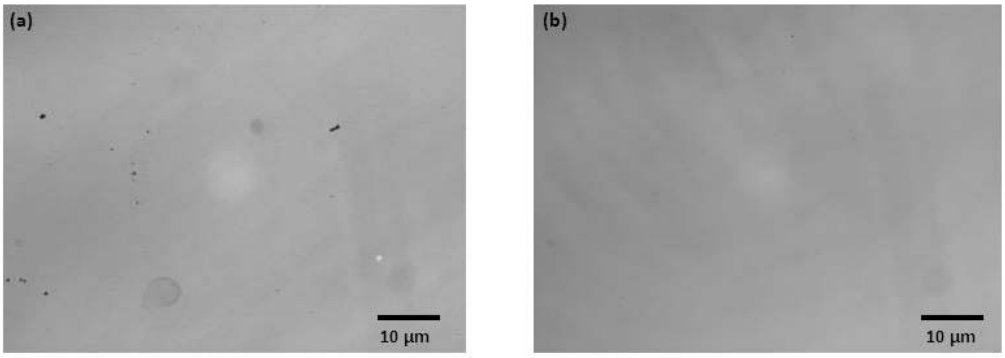

Figure 3.3 Optical surface image of polished oxide films by (a) ceria based slurry (b) nanodiamond-polymer based slurry

The oxide wafers were characterized by optical microscopy in order to investigate post-CMP surface quality by novel nanodiamond-polymer based slurry. The optical microscopic images of polished oxide films are shown in figure 3.3. It can be clearly observed that the scratches are present on the oxide surface in case of polishing by conventional ceria based slurry. On the contrary, the oxide wafer surface polished with novel nanodiamond polymer based slurry is devoid of scratches on the surface.

3.6 Summary

In summary, the novel nanodiamond polymer based slurry synthesized by co-polymerization of N-isopropylacrylamide (NIPAM) and N,N'-methylenebisacrylamide, 3-(trimethoxysilyl) propyl methacrylate (MPS) incorporating nanodiamond particles can become next generation environmentally benign slurry. The synthesized slurry and the commercial ceria based slurry were used to polish silicon dioxide films. The novel

synthesized slurry showed superior performance in terms of the surface finish. The TEM images have shown that the ceria nanoparticles are uniformly distributed without large amount of agglomeration in the film. The polishing of oxide wafers have utilized both the synthesized nanodiamond-polymer based slurry and conventional slurry for polishing the SiO_2 surface. The ceria based slurry is free of any oxidizers, however the slurry performance could be enhanced by adding suitable chemical additives. The oxide wafers were also characterized by optical microscopy in order to investigate post-CMP surface quality by novel nanodiamond-polymer based slurry. However, the material removal rate was lower in case of synthesized slurry than that of commercial ceria based slurry.

3.7 References

[1] Yuzhuo Li (Ed.), Microelectronic Application of Chemical Mechanical Planarization, ISBN978-0-471-71919-9, (2008).

[2] Parshuram B. Zantye, Ashok Kumar, A.K. Sikdar, 'Materials Science and Engineering R, Vol. 45 pp. 89-220 (2004).

[3] H. Gomez, M.K. Ram, F. Alvi, Elias Stefanakos, A. Kumar, Journal of Physical Chemistry C 144 (2010) 18797-18804.

[4] A.K. Sikder, A. Kumar, Journal of Electronic Materials, 31 (2002) 1016-1021.

[5] J.M. Steigerwald et. al., Chemical Mechanical Planarization of Microelectronic Materials, Wiley-Interscience Publications, ISBN 0-471-13827-4, (1997).

[6] Cecil Coutinho, Ph.D. Dissertaion, University of South Florida, 2009

CHAPTER 4

CMP OF COPPER FILMS

4.1 Introduction

Traditionally, aluminum had been used as interconnects in fabrication of multi-level device structures in spite of known advantageous properties of copper: Copper is a better conductor than aluminum and possesses better electromigration resistance than aluminum. The main reason for not using copper as interconnects was the non-existence of volatile copper compounds that can be used in the patterning by reactive ion etching (RIE) masking as in aluminum. After the establishment of tungsten plug technology, CMP played an important role in the transition from aluminum to copper interconnect for IC fabrication. Copper CMP has similar damascene structure as that of tungsten CMP and is schematically shown in figure 4.1[1].

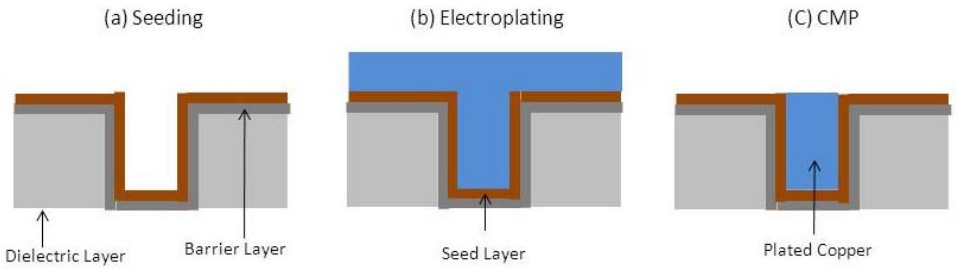

Figure 4.1 Damascene process [1]

In step 1, the pattering of dielectric is done by RIE followed by barrier layer deposition to present diffusion of copper into dielectric layer and subsequently copper is

deposited by electrochemical deposition (ECD). Lastly, as seen in figure 4.1c, excess copper is removed and surface is made flat using CMP process.

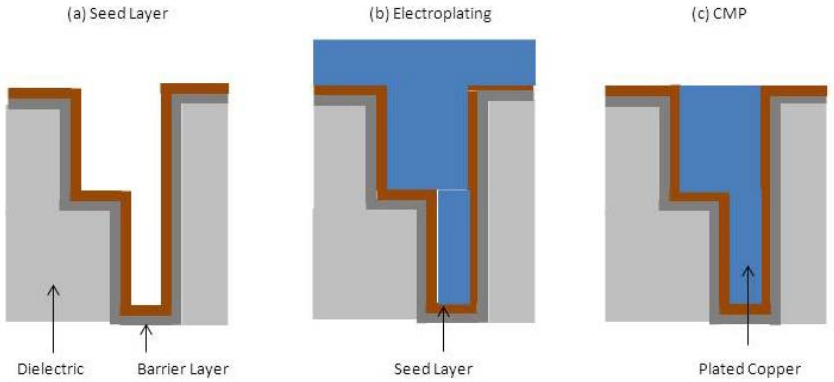

Figure 4.2 Dual Damascene process [1]

Copper serves the purpose of interconnect and wiring in the fabrication of multi-level structure as shown in figure 4.2 [1]. This process is called dual damascene which allows deposit in copper of via as well as in interconnect reducing the number steps in IC fabrication process. As a result of CMP, the current state-of-the-art IC fabrication is capable of 7-8 wiring level that was earlier limited to 3-4 wiring level (figure 1.1) with poor performance [2].

4.2 Synthesis of Copper Films

The copper coated wafers used in this research were procured from SEMATECH International. The copper thin films were deposited on silicon substrate by electrochemical deposition techniques in two steps. In the first step, a thin seed layer of copper was deposited on the silicon substrate followed by the deposition of bulk copper using electroplating. The thickness of copper coating thickness was 10 kÅ [3]. Electrochemical deposition technique of depositing copper films offers significant

advantage over chemical vapor deposition or physical vapor deposition in terms of cost efficiency [4].

4.3 CMP of Copper Films

The CMP of blanket copper wafers were performed by using CETR bench-top CMP tester (figure 2.16).Table 4.1 shows the input parameters used in the polishing of copper wafers. The selected input parameters were optimized in order to obtain best polished copper surface. The electroplated copper wafers with thickness 10 kÅ were prepared at SEMATECH International by electroplating technique. Several die having size of 20 mm × 20 mm were cut from 12 inch copper wafer, and used for polishing. In order to make edges of the die uniform, their edges were polished using diamond file.

Table 4.1 Input parameters for copper CMP

#	Parameter	Conditions
1	Down Pressure	2-4psi
2	Platen Rotation	150-250 RPM
3	Slider Position and Movement	45mm ± 5mm @ velocity of 5 mm/ sec
4	Slurry	Cabot 5001
5	Pad	Rodel, Inc. IC1000 Suba IV
6	Time of polishing	60 sec
7	Polishing Specimen	2 cm × 2 cm coupon

The sample was mounted onto the sample holder using 3M^{TM} double coated adhesive transfer tapes. The 6 inch polymeric Suba IV/ IC 1000 polishing pad (table 3.1) was used as a counter polishing material for copper samples. The standard commercial Cabot 5001 slurry mixed with 2% hydrogen peroxide was utilized for polishing process. Prior to the polishing of copper wafer, the polishing pad was conditioned for 20 minutes using diamond conditioner and deionized water. The actual polishing of copper wafer was done for 60 seconds. The removal rate was calculated by using formula describe in section 4.3.4, while surface roughness were analyzed by using AFM.

4.4 Results and Discussion

The effect of various input parameters such as pressure, relative speed were analyzed for blanket copper wafer. Figure 4.3, 4.4, and 4.6 show the real time coefficient of friction versus time graph, variation of removal rate with pressure at constant speed, and variation of removal rates with speed at constant pressure respectively. The removal rate was increased with increase in pressure and speed, which is approximately in concert with Preston's equation as described in section 2.4. The pressure variation is kept low because at higher pressure copper film tends to vanish quickly [5].

The standard commercial Cabot 5001 slurry mixed with hydrogen peroxide removes material by following actions.

- The mixture of a complexing agent and an oxidizer in the slurry oxidizes copper into soft porous copper oxide film.
- The soft porous copper oxide film is removed by mechanical action of abrasive particles present in the slurry and polishing pad.

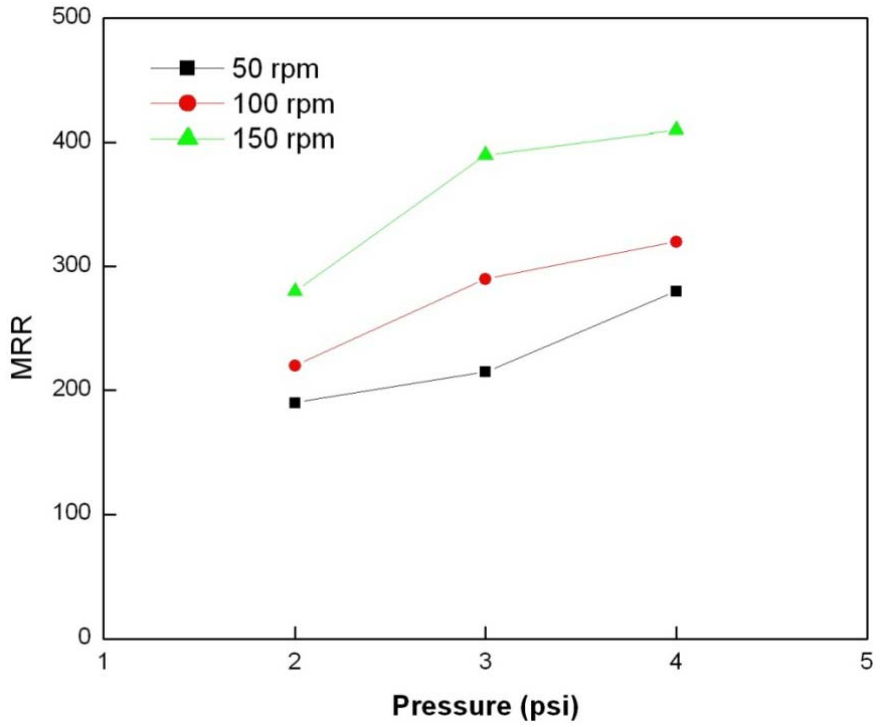

Figure 4.4 Material removal rate versus pressure following Preston's Law

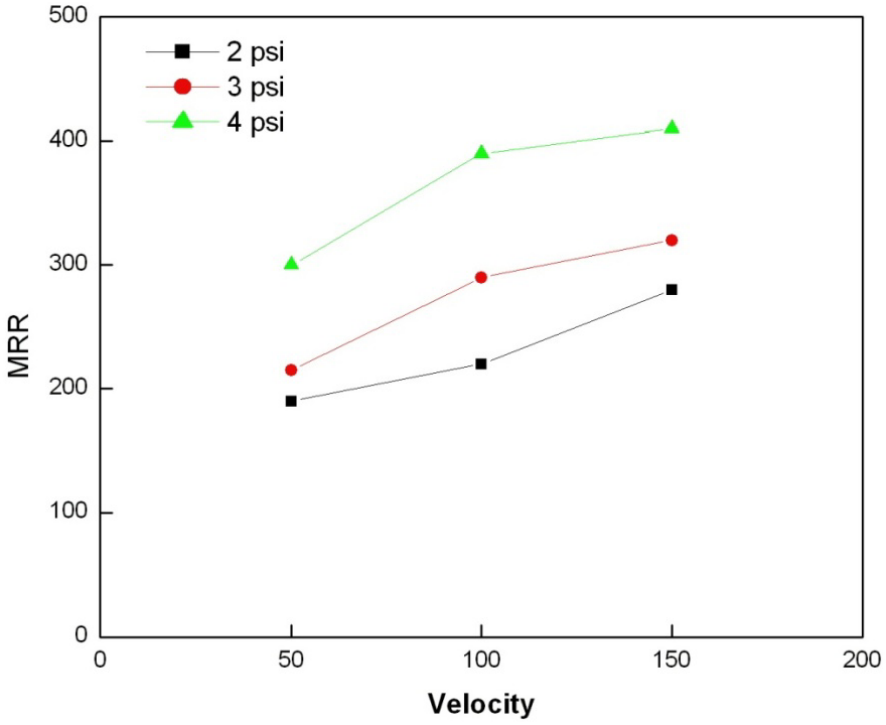

Figure 4.5 Material removal rate versus velocity following Preston's Law

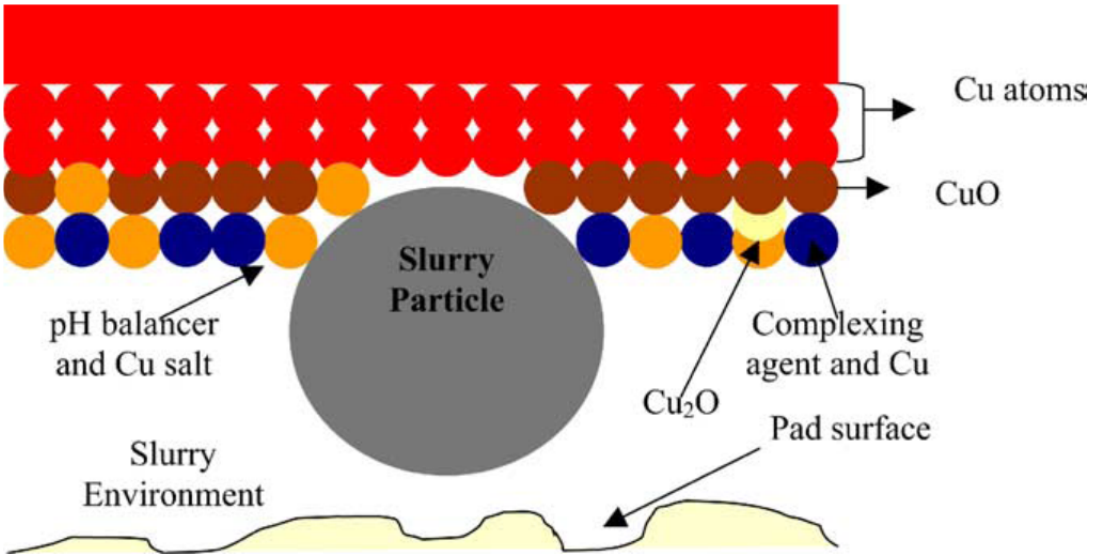

Figure 4.6 A representation of slurry interaction with copper surface [6]

The pH of the slurry was kept at a value of 6 in order to maximize removal rate. At this particular pH value, the copper film gets oxidized into soft porous oxide (CuO and Cu_2O) to facilitate mechanical material removal. This behavior can be understood using the Pourbaix diagram [7]. The schematic diagram of material removal mechanism of copper is depicted in figure 4.6, which shows the different phenomenon occurring at the surface of the copper wafer during polishing. The equation 7 and 8 proposed chemical reactions occur during the CMP of copper wafer [6].

The complexing agent combined with an oxidizer creates a soft porous copper oxide film on the surface of copper wafer, which can be easily removed by abrasives. In absence of the complexing agent, copper oxide film which is harder than copper prohibits desirable planarization effect [5]. This is highly inefficient for the CMP point of view, and that is why a tailored mixture of abrasives, an oxidizer, and a complexing agent

should constitute the slurry in order to produce optimal results. Figure 4.7 and 4.8 shows the copper wafer surface before and after polishing.

$$Cu_2^+ + 2e^- \leftrightarrow Cu \tag{7}$$

$$2Cu_2^+ + H_2O + 2e^- \leftrightarrow Cu_2O + 2H^+ \tag{8}$$

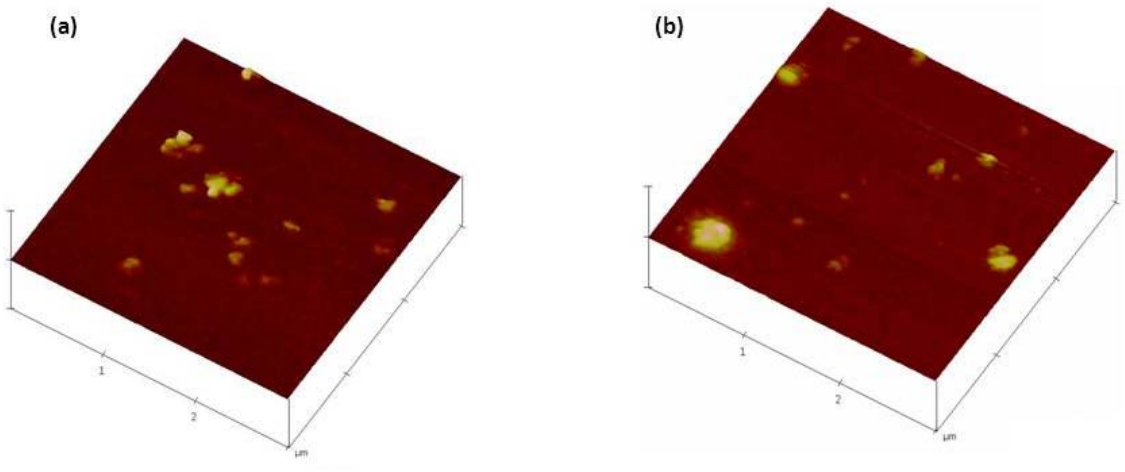

Figure 4.7 AFM surface image of copper film (a) before CMP with average surface roughness of 5.2 nm (b) after CMP with average surface roughness of 1.8 nm at 2 psi and 50 rpm.

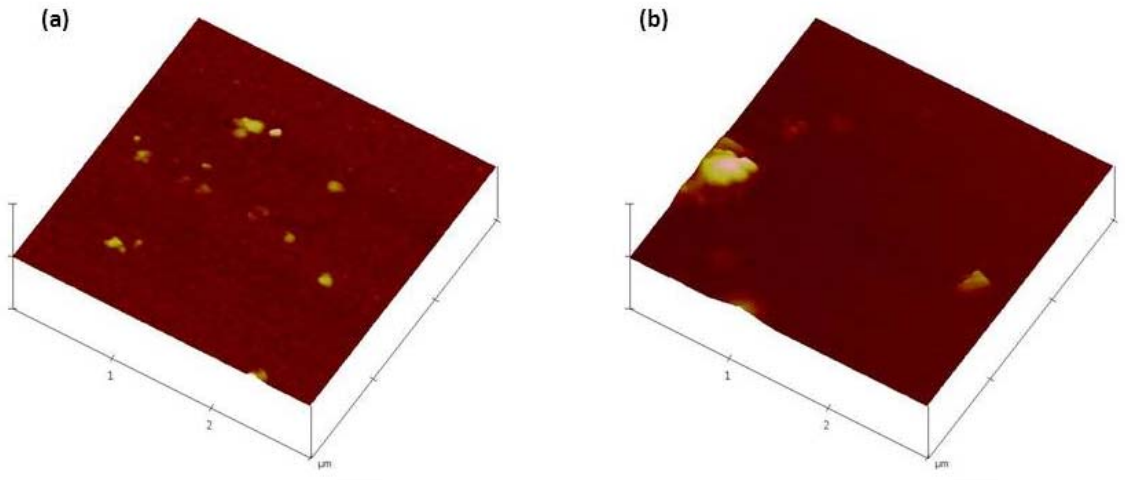

Figure 4.8 AFM surface image of copper film (a) before CMP with average surface roughness of 4.7 nm (b) after CMP with average surface roughness of 2.0 nm at 4 psi and 150 rpm

The average surface roughness of copper films was reduced from 4.7nm to 1.7 nm after polishing. The average surface roughness before polishing of copper films were found to be 4.9 nm, and after polishing the surface roughness found to be 1.2 nm. This represents significant decrease in the surface roughness during polishing. These results are also in lines with the results that reported in the literature [8].

4.5 Summary

The copper wafers were polishing and the process conditions were optimized in terms of velocity, pressure, and slurry flow rate. The commercial slurry was used to polish the copper wafers, and results showed significant decrease in surface roughness and superior surface finish with minimal scratches.

4.6 References

[1] Annabelle Pratt, Overview of the copper interconnects in the semiconductor industry, Advanced Energy Industries Inc.

[2] M.R. Oliver (Ed.), Chemical-Mechanical Planarization of Semiconductor Materials, Springer series in materials science, Vol. 69, 2004, ISBN 3-540-43181-0.

[3] A.K. Sikder, A. Kumar, Journal of Electronic Materials, 31 (2002) 1016-1021.

[4] Lavanya Sriram, M.S. Thesis, University of South Florida, 2004.

[5] Yuzhuo Li (Ed.), Microelectronic Application of Chemical Mechanical Planarization, ISBN978-0-471-71919-9, (2008).

[6] P. Zantye, A. Kumar, A.K. Sikdar, Materials Science and Engineering R, Vol. 45, (2004).

[7] Pourbaix. Atlas of Electrochemical Equilibria in Aqueous Solutions. Houston, TX: National Association of Corrosion Engineering; 1974.

[8] Subrahmanya R. Mudhivarthi, Ph.D. Dissertation, University of South Florida, 2007.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 CVD Diamond Films

5.1.1 Conclusion

In this research work, CVD diamond films were grown and characterized. These CVD diamond films were polished using CMP technique in order to reduce surface roughness. Based on the outcome, following conclusions are drawn:

- Optimized HFCVD technique by using Raman Spectroscopy on the synthesized samples established the process parameters for the highly quality diamond films deposition.
- Series of characterization techniques proved to be advantageous for CVD diamond films characterization.
- CMP process parameters were optimized in order to achieve optimum polish output
- Significant reduction in the surface roughness of the CVD diamond films is observed by CMP process.

5.1.2 Future Work

This work is limited in varying processing parameters during CMP process in terms of pressure, relative speed, slurry, and polishing pad. This work can be extended by using slurry consisting of strong oxidizer in order to further enhance material removal

rate. More sophisticated and advanced polishing pad could also aid in enhancing material removal rate. In addition, the detailed understanding of underlying material removal can be achieved by analyzing CVD diamond films using X-ray Photoelectron Spectroscopy (XPS) and/or Augur Electron Spectroscopy (AES).

5.2 Silicon Dioxide Films

5.2.1 Conclusion

Silicon dioxide films were polished using bench-top CMP tester under optimized conditions. The slurries used for polishing were traditional ceria nanoparticles based and novel nanodiamond polymer slurry. Following conclusion are drawn based on results obtained

- The novel slurry was successfully synthesized by co-polymerization of N-isopropylacrylamide (NIPAM) and N,N'-methylenebisacrylamide, 3-(trimethoxysilyl) propyl methacrylate (MPS) incorporating nanodiamond particles.
- The synthesized novel nanodiamond polymer based slurry showed uniform distribution of nanodiamond particles in the polymer matrix.
- The polishing performed using novel slurry showed high quality surface finish with minimal scratches than that achieved by polishing using conventional ceria based slurry.
- The output parameters of CMP process including material removal rate and coefficient of friction were analyzed in order study the change in tribological properties during polishing.

5.2.2 Future Work

The silicon dioxide CMP process is studied in details, but this study can be further enhanced by incorporating the polishing behavior of different low-k dielectric materials. The novel slurry can also be further tailored by using different nanoparticles like zirconia, silica to achieve optimum output.

5.3 Copper Films

5.3.1 Conclusion

The blanked copper wafers polished by using commercial slurry in CETR bench-top tester. Based on polished results, following conclusions are drawn:

- The material removal rate during copper polishing increased with increasing polishing velocity and pressure, thereby, closely satisfying Preston's law.
- The post-CMP characterization of copper films was performed by AFM and results showed significant reduction (4.7 nm 1.2 nm) to in the average surface roughness of copper film.

5.3.2 Future Work

The copper films were polished using the commercial slurry, this work can be further extended to synthesize the novel abrasive free slurry for copper polishing. This would involve the deeper understanding of copper CMP process in terms of role of various components present in the slurry like complexing agent, passivating agent, and surfactants.